#5A

KILLWORTH, GOTTMAN, HAGAN & SCHAEFF, L.L.P.
ATTORNEYS AT LAW
ONE DAYTON CENTRE
ONE SOUTH MAIN STREET, SUITE 500
DAYTON, OHIO 45402-2023
937/223-2050
FACSIMILE: 937/223-0724
EMAIL: KGHS@KGHS.COM

RICHARD A. KILLWORTH
JAMES F. GOTTMAN
TIMOTHY W. HAGAN
B. JOSEPH SCHAEFF
RICHARD C. STEVENS
ROBERT L. SHOWALTER
KIMBERLY GAMBREL

JODY H. ARMSTRONG
JAMES E. BEYER

BRADLEY A. KELLER
STEPHEN A. CALOGERO
CHARLOTTE L. BARNEY

PATENT AGENT
SUSAN M. LUNA

OF COUNSEL
DAVID A. SHOUGH

August 21, 1997

In re Application of **VIA EXPRESS MAIL** EI719015108US

Inventor(s) : Jigish D. Trivedi
Title : **LOW RESISTANCE METAL SILICIDE LOCAL INTERCONNECTS AND A METHOD OF MAKING**
Assignee : Micron Technology, Inc.
Docket No. : MIO 024 PA

Box PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed are the following papers:

__X__ Specification, abstract and claims, 31 pages total
__X__ Drawings 7 sheets (3 sets-formal)
__X__ Declaration and Power of Attorney
_____ A claim for priority under 35 USC §119 is hereby made with respect to _____ application No. _____ filed _____. A certified copy of that application _____ is enclosed/_____ will be filed later.
__X__ Recordation Form Cover Sheet, Assignment and separate check $40.00 (recordal fee)

Calculation of Fee

Basic Fee			$770.00
Total Claims	40 - 20 = 20 X $22.00	=	440.00
Independent Claims	13 - 3 = 10 X $80.00	=	800.00
Charge for Multiple dependent claims ($260.00)		=	- 0
	TOTAL		$2010.00

Enclosed are our checks in the amounts of $2010.00 and $40.00 which represent the payment of the above filing fees.

Respectfully submitted,
KILLWORTH, GOTTMAN, HAGAN & SCHAEFF, L.L.P.

By _____
Timothy W. Hagan
Reg. No. 29,001

JFG/SAC:nmm/Encls.

Attorney Docket No. - MIO024PA/97-0043

LOW RESISTANCE METAL SILICIDE LOCAL INTERCONNECTS AND A METHOD OF MAKING

BACKGROUND OF THE INVENTION

The present invention relates in general to a local interconnect, and, more particularly, to a low resistance local interconnect having a refractory metal silicide, and a process of making the same.

In the manufacture of integrated circuits used in the construction of dynamic random access memories (DRAMs), static random access memories (SRAMs), and the like, interconnects are required to provide the necessary electrical paths between field effect transistors and other devices fabricated on the semiconductor substrate and the external circuitry used to pass data to and from these devices. Polycide structures are commonly used to form the gate of a metal oxide semiconductor field effect transistor (MOSFET). Polycide structures are especially attractive for self-aligned gates. A polycide structure is formed by depositing a layer of doped polysilicon over the gate insulation layer. The polysilicon is then etched to define the gate electrode. A refractory metal, such as titanium, is then formed over the remaining polysilicon and silicon substrate. A metal silicide is formed by annealing the polysilicon and the refractory metal with the polysilicon supplying the source of silicon for the silicide. The unreacted refractory metal is etched, with the remaining polysilicon and metal silicide forming the polycide gate.

A local interconnect is typically used to connect the polycide gate to certain active semiconductor areas, such as the drain or source of another MOSFET. A local interconnect may also be used to connect active semiconductor areas to other active semiconductor areas which are separated by an insulating region, such as a field oxide region. Titanium silicide ($TiSi_2$) is commonly used as a local interconnect for connecting desired polycide gates and active semiconductor areas. $TiSi_2$ may be formed through physical vapor deposition (PVD) or chemical vapor deposition (CVD). PVD entails sputtering titanium followed by a layer of silicon. The titanium and silicon are reacted to

form $TiSi_2$. Silicon from the underlying areas also reacts with the titanium to form $TiSi_2$. CVD typically entails reacting titanium tetrachloride ($TiCl_4$) and silane (SiH_4) in the gas phase to form $TiSi_2$. Silicon from the underlying areas is also consumed in the CVD reaction to form $TiSi_2$.

While $TiSi_2$ is a relatively low resistive conductor, the titanium is susceptible to oxidation during and after its formation. The resultant titanium dioxide (TiO_2) increases the sheet resistance of the interconnect thereby increasing power dissipation and reducing the speed of the device. As used herein, sheet resistance is an electrical quantity measured on a thin layer and has the units of ohms/square. Further, a layer of TiO_2 makes it difficult to form good electrical contacts on the $TiSi_2$ interconnect and poses adhesion problems when subsequent layers are deposited on top of the interconnect line. Further, $TiSi_2$ is susceptible to damage during subsequent contact formation as the typical contact etch also consumes $TiSi_2$. Typically, the size of the interconnect must be increased in order to compensate for damage caused by the contact etch.

Accordingly, there is a need for a local interconnect having a lower resistance and one in which the effects of oxidation are reduced. Preferably, the local interconnect is smaller in width and thickness. There is also a need for a method of forming such a local interconnect. Preferably, such a method would be inexpensive, easy to implement and would not entail excess processing steps.

SUMMARY OF THE INVENTION

The present invention meets these needs by providing a local interconnect formed by a process in which a layer of metal silicide serves both as a hard mask and source of silicon for an underlying layer of metal. The metal silicide is patterned to form the boundaries of the local interconnect and then reacted with the underlying layer of metal. Silicon from the metal silicide combines with the underlying metal to form another metal silicide. An intermetallic compound comprised of metal from the underlying metal layer and metal from the metal silicide is also formed. Unreacted

metal from the underlying metal layer is removed to form the local interconnect. The metal silicide also serves as a contact etch stop during subsequent contact formation thereby allowing for a smaller local interconnect.

According to a first aspect of the present invention, a process of forming a local interconnect comprises providing at least one semiconductor layer. A layer of metal is formed over the at least one semiconductor layer. A contact etch stop is formed over the layer of metal. The layer of metal is reacted with the contact etch stop and then the unreacted metal is removed from the layer of metal to form the local interconnect. The contact etch stop may comprise a metal silicide. The process may further comprise the step of patterning the contact etch stop to form the boundaries of the local interconnect. The step of patterning the contact etch stop to form the boundaries of the local interconnect may be performed prior to the step of reacting the layer of metal with the contact etch stop.

According to another aspect of the present invention, a process of forming a local interconnect comprises providing at least one semiconductor layer. A layer of metal is formed over the at least one semiconductor layer. A layer of metal silicide is formed over the layer of metal. The layer of metal silicide is reacted with the layer of metal, and then unreacted metal remaining from the layer of metal is removed to form the local interconnect. The layer of metal may comprise a refractory metal selected from the group consisting of chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium, tungsten, and vanadium. Preferably, the refractory metal comprises titanium. The layer of metal may have a thickness in the range of about 200 Angstroms to about 600 Angstroms, and preferably, approximately 300 Angstroms. The layer of metal silicide may comprise tungsten silicide. The layer of metal silicide may have a thickness in the range of about 500 Angstroms to about 1200 Angstroms, and preferably, in the range of about 600 Angstroms to about 700 Angstroms. The step of reacting the layer of metal silicide with the layer of metal may comprise annealing the layer of metal silicide and the layer of metal at a temperature ranging from about 600°C to about 700°C.

According to yet another aspect of the present invention, a process of forming a local interconnect comprises providing at least one semiconductor layer. A layer of metal is formed over the at least one semiconductor layer by chemical vapor deposition (CVD). A layer of metal silicide is formed over the layer of metal by CVD. The layer of metal silicide is then patterned. The metal silicide is reacted with the layer of metal and then unreacted metal remaining from the layer of metal is removed to form the local interconnect. The step of forming a layer of metal over the at least one semiconductor layer by CVD and the step of forming a layer of metal silicide over the layer of metal by CVD are preferably carried out in the same vacuum environment.

According to a further aspect of the present invention, a process of forming a local interconnect comprises providing at least one semiconductor layer. A layer of metal is formed over the at least one semiconductor layer. A layer of first metal silicide is formed over the layer of metal. The layer of first metal silicide and the layer of metal are annealed to form a composite structure. Remaining metal from the layer of metal is removed to form the local interconnect. The composite structure may comprise the first metal silicide, a second metal silicide and an intermetallic compound comprising metal from the layer of metal and metal from the first metal silicide. The layer of metal may comprise titanium and the first metal silicide may comprise tungsten silicide, such that the composite structure comprises tungsten silicide, titanium silicide, and titanium tungsten intermetallic compound. The process may further comprise the step of patterning the layer of first metal silicide to form a boundary of the local interconnect. The step of patterning the layer of first metal silicide to form a boundary of the local interconnect is preferably performed prior to the step of annealing the layer of first metal silicide and the layer of metal to form a composite structure.

According to a still further aspect of the present invention, a process of forming a local interconnect comprises providing at least one semiconductor layer. A layer of refractory metal is formed over the at least one semiconductor layer. A layer of first metal silicide is formed over the layer of refractory metal. The layer of first metal silicide is patterned to define a boundary of the local interconnect. The patterned first metal

silicide and the layer of refractory metal are annealed to form a composite structure. Refractory metal remaining from the layer of refractory metal is removed to form the local interconnect. The step of patterning the layer of first metal silicide to define a boundary of the local interconnect may comprise the step of selectively etching the layer of first metal silicide. The step of selectively etching the layer of first metal silicide may comprise the step of dry etching the layer of first metal silicide. The step of annealing the patterned first metal silicide and the layer of refractory metal to form a composite structure is preferably carried out in an atmosphere of reactive nitrogen such that at least refractory metal remaining from the layer of refractory metal is nitrified.

According to another aspect of the present invention, a process of forming a local interconnect comprises providing at least one semiconductor layer. A layer of titanium having a thickness ranging from about 200 Angstroms to about 600 Angstroms is formed over the at least one semiconductor layer. A mask layer of tungsten silicide having a thickness ranging from about 500 Angstroms to about 1200 Angstroms is formed over the layer of titanium. The mask layer is selectively etched to define a boundary of the local interconnect. The mask layer and the layer of titanium are annealed in an atmosphere of reactive nitrogen thereby forming a composite structure of titanium silicide, tungsten silicide and a titanium tungsten intermetallic compound where the mask layer contacts the layer of titanium. The layer of titanium not covered by the mask layer is nitrified to form a layer of titanium nitride. The layer of titanium nitride and underlying titanium is then removed to form the local interconnect.

According to yet another aspect of the present invention, a process of forming a semiconductor device comprises providing a substrate assembly having at least one semiconductor layer. Source and drain regions of a field effect transistor are formed in the at least one semiconductor layer. A gate oxide is formed over the at least one semiconductor layer. A gate contact is formed over the gate oxide. A layer of refractory metal is formed over the at least one semiconductor layer. A layer of first metal silicide is formed over the layer of metal. The layer of first metal silicide is patterned to define a boundary of a local interconnect. The layer of refractory metal

and the layer of first metal silicide are annealed to form a composite structure. Remaining refractory metal from the layer of refractory metal is removed to form the local interconnect. The local interconnect connects at least one of the source, drain, and gate to another active area within the substrate assembly.

According to a further aspect of the present invention, a process of forming a memory array having a plurality of memory cells arranged in rows and columns with each of the plurality of memory cells comprising at least one field effect transistor comprises providing at least one semiconductor layer. Sources, drains and gates for each of the field effect transistors are formed over the at least one semiconductor layer. A layer of refractory metal is formed over the at least one semiconductor layer. A layer of first metal silicide if formed over the layer of refractory metal. The layer of first metal silicide is patterned to define a boundary of at least one local interconnect. The layer of refractory metal and the layer of first metal silicide are annealed to form a composite structure. Remaining metal from the layer of refractory metal is removed to form the at least one local interconnect. The at least one local interconnect connects at least one of the source, drain and gate of one of the field effect transistors with another active area of the memory array.

According to a yet still further aspect of the present invention, a process of fabricating a wafer comprises providing a wafer having a substrate assembly. The substrate assembly has at least one semiconductor layer. A repeating series of sources, drains and gates for at least one field effect transistor on each of a plurality of individual die on the wafer are formed over the at least one semiconductor layer. A layer of refractory metal is formed over the at least one semiconductor layer. A layer of first metal silicide is formed over the layer of refractory metal. The layer of first metal silicide is patterned to define a boundary of at least one local interconnect in each of the individual die. The layer of refractory metal and the layer of first metal silicide are annealed to form a composite structure and refractory metal remaining from the layer of refractory metal is removed to form the at least one local interconnect in each of the individual die. The at least one local interconnect in each of the individual die connect

at least one of the source, drain and gate of one of the field effect transistors with another active area in each of the individual die.

According to a further aspect of the present invention, a local interconnect comprises a composite structure. The composite structure comprises a first metal silicide, a second metal silicide and an intermetallic compound comprising metal from the first metal silicide and metal from the second metal silicide. The first metal silicide and the second metal silicide preferably each comprise at least one refractory metal. The at least one refractory metal for the first metal silicide and the second metal silicide are selected from the group consisting of chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium, tungsten, and vanadium. Preferably, the first metal silicide comprises titanium silicide and the second metal silicide comprises tungsten silicide.

According to a still further aspect of the present invention, a local interconnect for connecting a first active semiconductor region to a second active semiconductor region on a substrate assembly with the first and second active semiconductor regions being separated by an insulating region comprises a composite structure. The composite structure comprises a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from the first refractory metal silicide and refractory metal from the second refractory metal silicide. The refractory metal from the first refractory metal silicide is different from the refractory metal from the second refractor metal silicide. The composite structure preferably has a thickness in the range of about 700 Angstroms to about 1800 Angstroms.

According to another aspect of the present invention, a semiconductor device comprises a substrate assembly having at least one semiconductor layer. At least one field effect transistor is formed in the at least one semiconductor layer with the least one field effect transistor having a source, a drain and a gate. The semiconductor device further comprises a local interconnect for connecting at least one of the source, the drain and the gate to another active area within the substrate assembly. The local interconnect comprises a composite structure comprising a first refractory metal silicide,

a second refractory metal silicide and an intermetallic compound comprising refractory metal from the first refractory metal silicide and refractory metal from the second refractory metal silicide.

According to a yet still further aspect of the present invention, a memory array comprises a plurality of memory cells arranged in rows and columns and formed on a substrate assembly having at least one semiconductor layer. Each of the plurality of memory cells comprises at least one field effect transistor and at least one local interconnect for connecting at least one of a source, a drain and a gate of the at least one field effect transistor in one of the plurality of memory cells to one of an active area within the one memory cell or to one of a source, a drain and a gate of the at least one field effect transistor in another one of the plurality of memory cells. The local interconnect comprises a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from the first refractory metal silicide and refractory metal from the second refractory metal silicide. The memory array may further comprise a plurality of local interconnects for connecting additional active areas within each of the plurality of memory cells. The memory array may also further comprise a plurality of local interconnects for connecting together active areas from different memory cells.

Accordingly, it is an object of the present invention to provide a low resistance local interconnect by a process in which a layer of metal silicide serves both as a mask and contact etch stop. Another aspect of the present invention is to provide a local interconnect which is smaller in width and thickness. Yet another object of the present invention is to provide a process of forming a local interconnect in which the negative effects of oxidation are reduced. It is a further object of the present invention to provide a process of forming a local interconnect which is inexpensive, easy to implement, and does not entail excess processing steps.

Other features and advantages of the invention will be apparent from the following description, the accompanying drawings and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-2 are enlarged, sectioned side views depicting the formation of a MOSFET for interconnection according to an aspect of the present invention;

Figs. 3-7 are enlarged, sectional side views depicting the formation of a local interconnect according to an aspect of the present invention;

Fig. 8 is a schematic diagram of an integrated circuit with a pair of CMOS inverters interconnected by the local interconnect of Fig. 7;

Fig. 9 is a schematic diagram of an SRAM array having a plurality of memory cells arranged in rows and columns;

Fig. 9A is a schematic diagram of a representative memory cell of the SRAM array of Fig. 9 with the local interconnect of Fig. 7;

Fig. 10 is a schematic diagram of a DRAM array having a plurality of memory cells arranged in rows and columns;

Fig. 10A is a schematic diagram of a representative memory cell of the DRAM array of Fig. 10 with the local interconnect of Fig. 7; and

Fig. 11 is a top view of a wafer having the local interconnect of Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to Fig. 1, a substrate assembly 10 is shown. The substrate assembly 10 comprises a semiconductor layer 12, which is silicon in the illustrated embodiment, and may also include additional layers or structures which define active or operable portions of semiconductor devices (not shown). For example, the semiconductor layer 12 of the substrate assembly 10 may be formed on insulating material, sapphire or another base material. The semiconductor layer 12 is doped with impurities to form a semiconductor of a first/p-type conductivity, or a second/n-type conductivity.

A number of different semiconductor devices may be formed on the semiconductor layer 12. In the illustrated embodiment, a metal oxide semiconductor field effect transistor (MOSFET) 14 having a self-aligned gate (G) is formed. It will be

appreciated by those skilled in the art that the term MOSFET is a generic term for any field effect transistor in which a conductive material is formed over the gate insulating material of a field effect transistor. The MOSFET 14 having the self-aligned gate (G) may be formed in accordance with the process described in copending application, U.S. Serial No. 08/858,772 (Attorney Docket No. MIO 010 PA), A METHOD OF FORMING A FIELD EFFECT TRANSISTOR HAVING A SELF-ALIGNED GATE, filed 5/20/97, by Donahoe et al., herein incorporated by reference. Another method of forming the MOSFET 14 comprises the following steps. The MOSFET 14 is isolated by a pair of field oxide regions 16. A gate insulation layer 18 is formed over the semiconductor layer 12 to a thickness of about 50 Angstroms to about 500 Angstroms depending on the device type and function. The field oxide regions 16 and the gate insulation layer 18 are comprised of silicon dioxide in the illustrated embodiment. A layer of polysilicon 20 is formed over the gate insulation layer 18 to a thickness of approximately 4000 Angstroms. The layer of polysilicon 20 may be doped with impurities, such as phosphorous or boron, either in situ or after the layer 20 is formed, to increase its conductivity. A photoresist pattern 22 is then used to define the gate (G). The exposed portions of polysilicon 20 are then removed using conventional etching techniques along with the photoresist pattern 22.

As shown in Fig. 2, an implant is added to the semiconductor layer 12 in order to form a lightly doped drain. In the illustrated embodiment, an n-type lightly doped section 24 is formed in the semiconductor layer 12 and is aligned with the lateral edges of the polysilicon layer 20. A proper dopant, such as phosphorus, is ion implanted into the semiconductor layer 12 to form the n-type lightly doped section 24. It will be appreciated by those skilled in the art that other methods may be used to deposit the dopant into the semiconductor layer 12. A layer of silicon dioxide is formed over the semiconductor layer 12 and anisotropically etched to form spacers 26 on the sides of the polysilicon 20. Another proper dopant is ion implanted into the semiconductor layer 14 to form an n+ source (S) and an n+ drain (D) with the spacers 26 acting as ion masks. It will be appreciated by those skilled in the art that the source (S) and the drain

(D) terminals of a MOS transistor are typically identical with the drain/source label being applied for descriptive purposes once a voltage is applied to the transistor. For example, for n-type MOSFETs, the drain designation is applied to the terminal having the higher voltage potential with the source designation being applied to the other terminal. An anneal is then performed to repair the crystal damage caused by the ion implants and to electrically activate the dopants. It will be appreciated by those skilled in the art that the source (S) and the drain (D) may be formed by diffusion or epitaxy. The exposed portion of the gate insulation layer 18 is then removed thereby exposing the source (S) and drain (D) of the MOSFET 14. The source (S), drain (D) and gate (G) are active semiconductor areas for producing desired electronic functions. It will be appreciated by those skilled in the art that other active semiconductor areas, such as diodes, bipolar transistors, resistors, capacitors, and the like, may be formed on the semiconductor layer 12.

The resistance of the gate (G) is further reduced by forming a polycide gate contact 28. As described above, a refractory metal, such as titanium, is formed over the polysilicon 20. Titanium silicide 30 is then formed by reacting the titanium with the polysilicon 20 by annealing the same at an appropriate temperature for an appropriate period of time. The polycide gate contact 28 may then be interconnected with other active semiconductor areas as desired.

Figs. 3-6 show a local interconnect fabrication process according to an aspect of the present invention. In the illustrated embodiment, the drain (D) of the MOSFET 14 is connected to the source (S') of another MOSFET 14' formed adjacent to the MOSFET 14. The MOSFET 14' is formed using the same process described above with respect to the MOSFET 14. It should be apparent that other active semiconductor areas may be interconnected, such as the polycide gate contacts 28 of a number of different MOSFETs, or a gate (G) of one MOSFET to the drain (D) or the source (S) of another MOSFET. Further, other active semiconductor areas, such as a pair of diodes, may be interconnected with the local interconnect as described herein.

Referring specifically to Fig. 3, a layer of metal 32, such as titanium, is formed over the semiconductor layer 12 to a thickness ranging from about 200 Angstroms to about 600 Angstroms, and preferably about 300 Angstroms. The layer of Ti 32 may be formed by sputtering Ti using physical vapor deposition (PVD) at a temperature ranging from about 300°C to about 500°C for a predetermined period of time. The layer of Ti 32 may also be formed using chemical vapor deposition (CVD) at a temperature ranging from about 600°C to about 700°C, and typically from about 625°C to about 650°C, for a predetermined period of time. It should be apparent that the predetermined periods of time are dependent in part on the temperature selected for each of the above deposition methods. It will be appreciated by those skilled in the art that other deposition methods may be used to form the layer of Ti 32.

A layer of first metal silicide 34, such as tungsten silicide (WSi_x), is formed over the layer of Ti 32 to a thickness ranging from about 500 Angstroms to about 1200 Angstroms, and preferably from about 600 Angstroms to about 700 Angstroms. In the illustrated embodiment, the layer of WSi_x 34 is formed using CVD by reacting tungsten hexafluoride (WF_6) with silane (SiH_4) in the gas phase at a temperature ranging from about 350°C to about 450°C. It will be appreciated by those skilled in the art that other deposition methods may be used to form the layer of WSi_x 34. However, formation of the layer of Ti 32 and the layer of WSi_x 34 using CVD allows the layers to be formed in the same deposition chamber and vacuum environment, thereby simplifying the manufacturing process as the wafer does not have to be transferred between different chambers. Further, the negative effects of oxidation are reduced as the wafer is maintained in the same vacuum environment during formation of the layer of Ti 32 and the layer of WSi_x 34.

The boundary of the local interconnect is then defined through photolithography. A layer of photoresist 36 is formed over the layer of WSi_x 34 and patterned using conventional methods as shown in Fig. 4. Referring now to Fig. 5, the exposed portions of the WSi_x 34 are removed using a selective dry etch, thereby forming a patterned WSi_x structure 34A. The selective etch removes the WSi_x but does not affect

the underlying layer of Ti 32. The remaining photoresist 36 is removed using conventional methods with the remaining patterned WSi_x structure 34A defining the boundaries of the local interconnect. The WSi_x therefore serves as a hard mask for the local interconnect as the WSi_x may be selectively etched without removing any of the underlying Ti.

The patterned WSi_x structure 34A is reacted with the layer of Ti 32 by annealing the same at a temperature ranging from about 600°C to about 700°C in an atmosphere of reactive nitrogen, such as N_2 gas. The anneal may comprise a rapid thermal anneal (RTA) or a rapid thermal process (RTP). The anneal is performed in an oxygen free environment to prevent the formation of any undesired oxide layer. As shown in Fig. 6, a composite structure 37 is formed. The composite structure 37 comprises a second metal silicide as the underlying layer of Ti 32 in contact with the patterned WSi_x structure 34A is converted to $TiSi_2$. The patterned WSi_x structure 34A serves as the source of silicon for converting the underlying layer of Ti 32 to $TiSi_2$. The composite structure also includes an intermetallic compound or alloy of Ti W as well as the remaining WSi_x. The intermetallic compound of Ti W reduces the resistance of the local interconnect while also increasing its adhesion characteristics. The composite structure 37 has a thickness ranging from about 700 Angstroms to about 1800 Angstroms. A thin layer of titanium nitride (TiN) 38 is also formed in the uncovered portions of Ti as the reactive nitrogen reacts with the exposed Ti. Some of the Ti also reacts with the underlying silicon as the active semiconductor areas are silicided. As most active semiconductor areas are typically silicided to increase conductivity, the present invention allows for the formation of the local interconnect while siliciding the active semiconductor areas in a single set of processing steps.

As shown in Fig. 7, the unreacted Ti and the layer of TiN 38 are selectively removed with the composite structure 37 forming the local interconnect. Therefore, the composite structure 37 and the local interconnect, along with the reference number, may be used interchangeably. In the illustrated embodiment, a selective wet etch is used to remove the TiN and the Ti without affecting the composite structure 37.

Additional local interconnects may be formed using the above process so that the desired electronic configuration is achieved. Further, additional processing steps, such as metalization layers, insulating layers, passivating layers, and the like, may be added. During subsequent contact formation, the WSi_x acts as a contact etch stop. Once all of the desired connections and layers are formed, contacts must be added to connect the electronic device to external pins. The prior art $TiSi_2$ local interconnect was damaged during the contact etch as $TiSi_2$ is susceptible to the etch. However, the contact etch stops at WSi_x, thereby protecting the underlying $TiSi_2$ as the WSi_x does not react with the contact etch. Accordingly, the size of the local interconnect may be reduced as no damage is caused to the $TiSi_2$ during the contact etch.

While in the illustrated embodiment, titanium is the metal selected to form the layer of metal 32, it will be appreciated by those skilled in the art that other metals, particularly, refractory metals, such as chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, tungsten, and vanadium, may be used to form the layer of metal 32. Further, while tungsten silicide was used to form the layer of first metal silicide 34, it will be appreciated by those skilled in the art that other metals, particularly, refractory metals, such as chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium and vanadium, may be used as the metal to form the first metal silicide 34.

As shown schematically in Fig. 8, one or more of the local interconnects 37 may be used to connect various structures in an integrated circuit 40, such as the gates of two or more transistors 14, and respective sources to respective drains. One or more of the local interconnects 37 may also be used in a typical static random access memory (SRAM) array 42 or in a typical dynamic random access memory (DRAM) array 44, as shown in Figs. 9 and 10. The SRAM array 42 and the DRAM array 44 comprise a plurality of memory cells 46 arranged in rows and columns. Each of the memory cells 46 also comprise at least one transistor 14. By way of example and as shown in Fig. 9A, each of the memory cells 46 of the SRAM array 42 comprise a pair of access transistors 14, the gates of which are coupled to a respective row line 48 via the

local interconnect 37 of Fig. 7. Similarly, as shown in Fig. 10A, each of the memory cells 46 of the DRAM array 44 comprise a switch transistor 14, the gate of which is coupled to a respective word line 50 via the local interconnect 37 of Fig. 7. It should be apparent that the configuration of the local interconnects 37 is dependent, in part, on the desired interconnection of the gates of the transistors 14 as well as the interconnection of the sources and drains of the transistors 14. It should also be apparent that other devices within the integrated circuit 40, the SRAM array 42 and the DRAM array 44, such as external contacts, other FET transistors, bipolar transistors, resistors, capacitors, and the like, may be interconnected via the local interconnect 37. It should therefore be apparent that the local interconnect 37 is not limited to connections including the active areas of MOSFETs but may include connections to the other components listed above without connecting to the active areas of a MOSFET. The local interconnect 37 may also be used in the fabrication of a wafer W as shown in Fig. 10. The wafer W includes a plurality of individual dies 52. Wafer masks (not shown) are used to apply a desired circuit structure on each of the individual dies 52. The desired circuit structure may comprise any of the above described structures, i.e. the integrated circuit 40, the SRAM array 42 or the DRAM array 44, with the appropriate local interconnects 37. The wafer W is processed using standard wafer fabrication techniques.

Having described the invention in detail and by reference to preferred embodiments thereof, it will be apparent that modifications and variations are possible without departing from the scope of the invention defined in the appended claims.

CLAIMS

What is claimed is:

1. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of metal over said at least one semiconductor layer;

forming a contact etch stop over said layer of metal;

reacting said layer of metal with said contact etch stop; and

removing unreacted metal from said layer of metal to form said local interconnect.

2. The process of claim 1, wherein said contact etch stop comprises a metal silicide.

3. The process of claim 1, further comprising the step of patterning said contact etch stop to form the boundaries of said local interconnect.

4. The process of claim 3, wherein said step of patterning said contact etch stop to form the boundaries of said local interconnect is performed prior to said step of reacting said layer of metal with said contact etch stop.

5. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of metal over said at least one semiconductor layer;

forming a layer of metal silicide over said layer of metal;

reacting said layer of metal silicide with said layer of metal; and

removing unreacted metal remaining from said layer of metal to form said local interconnect.

6. The process of claim 5, wherein said layer of metal comprises a refractory metal.

7. The process of claim 6, wherein said refractory metal is selected from the group consisting of chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium, tungsten, and vanadium.

8. The process of claim 7, wherein said refractory metal comprises titanium.

9. The process of claim 5, wherein said layer of metal has a thickness in the range of about 200 Angstroms to about 600 Angstroms.

10. The process of claim 9, wherein said layer of metal has a thickness of approximately 300 Angstroms.

11. The process of claim 5, wherein said layer of metal silicide comprises tungsten silicide.

12. The process of claim 5, wherein said layer of metal silicide has a thickness in the range of about 500 Angstroms to about 1200 Angstroms.

13. The process of claim 12, wherein said layer of metal silicide has a thickness in the range of about 600 Angstroms to about 700 Angstroms.

14. The process of claim 5, wherein said step of reacting said layer of metal silicide with said layer of metal comprises annealing said layer of metal silicide and said layer of metal at a temperature ranging from about 600°C to about 700°C.

15. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of metal over said at least one semiconductor layer by chemical vapor deposition (CVD);

forming a layer of metal silicide over said layer of metal by CVD;

patterning said layer of metal silicide;

reacting said metal silicide with said layer of metal; and

removing unreacted metal remaining from said layer of metal to form said local interconnect.

16. The process of claim 15, wherein said step of forming a layer of metal over said at least one semiconductor layer by CVD and said step of forming a layer of metal silicide over said layer of metal by CVD are carried out in the same vacuum environment.

17. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of metal;

annealing said layer of first metal silicide and said layer of metal to form a composite structure; and

removing remaining metal from said layer of metal to form said local interconnect.

18. The process of claim 17, wherein said composite structure comprises said first metal silicide, a second metal silicide and an intermetallic compound comprising metal from said layer of metal and metal from said first metal silicide.

19. The process of claim 18, wherein said layer of metal comprises titanium and said first metal silicide comprises tungsten silicide, such that said composite structure comprises tungsten silicide, titanium silicide, and titanium tungsten intermetallic compound.

20. The process of claim 17, further comprising the step of patterning said layer of first metal silicide to form a boundary of said local interconnect.

21. The process of claim 20, wherein said step of patterning said layer of first metal silicide to form a boundary of said local interconnect is performed prior to said step of annealing said layer of first metal silicide and said layer of metal to form a composite structure

22. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of refractory metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of refractory metal;

patterning said layer of first metal silicide to define a boundary of said local interconnect;

annealing said patterned first metal silicide and said layer of refractory metal to form a composite structure; and

removing remaining refractory metal from said layer of refractory metal to form said local interconnect.

23. The process of claim 22, wherein said step of patterning said layer of first metal silicide to define a boundary of said local interconnect comprises the step of selectively etching said layer of first metal silicide.

24. The process of claim 23, wherein said step of selectively etching said layer of first metal silicide comprises the step of dry etching said layer of first metal silicide.

25. The process of claim 22, wherein said step of annealing said patterned first metal silicide and said layer of refractory metal to form a composite structure is carried out in an atmosphere of reactive nitrogen such that at least remaining refractory metal from said layer of refractory metal is nitrified.

26. A process of forming a local interconnect comprising:

providing at least one semiconductor layer;

forming a layer of titanium over said at least one semiconductor layer, said layer of titanium having a thickness ranging from about 200 Angstroms to about 600 Angstroms;

forming a mask layer of tungsten silicide over said layer of titanium, said mask layer of tungsten silicide having a thickness ranging from about 500 Angstroms to about 1200 Angstroms;

selectively etching said mask layer to define a boundary of said local interconnect;

annealing said mask layer and said layer of titanium in an atmosphere of reactive nitrogen thereby forming a composite structure where said mask layer contacts said layer of titanium and nitrifying at least said layer of titanium not covered by said mask layer to form a layer of titanium nitride, said composite structure comprising titanium silicide, tungsten silicide and a titanium tungsten intermetallic compound; and

removing said layer of titanium nitride and underlying titanium to form said local interconnect.

27. A process of forming a semiconductor device comprising:

providing a substrate assembly having at least one semiconductor layer;

forming source and drain regions of a field effect transistor in said at least one semiconductor layer;

forming a gate oxide over said at least one semiconductor layer;

forming a gate contact over said gate oxide;

forming a layer of refractory metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of metal;

patterning said layer of first metal silicide to define a boundary of a local interconnect;

annealing said layer of refractory metal and said layer of first metal silicide to form a composite structure; and

removing remaining refractory metal from said layer of refractory metal to form said local interconnect.

28. The process of claim 27, wherein said local interconnect connects at least one of said source, drain, and gate to another active area within said substrate assembly.

29. A process of forming a memory array, said memory array comprising a plurality of memory cells arranged in rows and columns, each of said plurality of memory cells comprising at least one field effect transistor, said process comprising:

providing at least one semiconductor layer;

forming sources, drains and gates for each of said field effect transistors over said at least one semiconductor layer;

forming a layer of refractory metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of refractory metal;

patterning said layer of first metal silicide to define a boundary of at least one local interconnect;

annealing said layer of refractory metal and said layer of first metal silicide to form a composite structure; and

removing remaining metal from said layer of refractory metal to form said at least one local interconnect, said at least one local interconnect connecting at least one of said source, drain and gate of one of said field effect transistors with another active area of said memory array.

30. A process of fabricating a wafer comprising:

providing a wafer having a substrate assembly, said substrate assembly having at least one semiconductor layer;

forming a repeating series of sources, drains and gates for at least one field effect transistor on each of a plurality of individual die on said wafer over said at least one semiconductor layer;

forming a layer of refractory metal over said at least one semiconductor layer;

forming a layer of first metal silicide over said layer of refractory metal;

patterning said layer of first metal silicide to define a boundary of at least one local interconnect in each of said individual die;

annealing said layer of refractory metal and said layer of first metal silicide to form a composite structure; and

removing remaining refractory metal from said layer of refractory metal to form said at least one local interconnect in each of said individual die, said at least one local interconnect in each of said individual die connecting at least one of said source, drain and gate of one of said field effect transistors with another active area in each of said individual die.

31. A local interconnect comprising:

a composite structure comprising a first metal silicide, a second metal silicide and an intermetallic compound comprising metal from said first metal silicide and metal from said second metal silicide.

32. The local interconnect of claim 31, wherein said first metal silicide and said second metal silicide each comprise at least one refractory metal.

33. The local interconnect of claim 32, wherein said at least one refractory metal for said first metal silicide and said second metal silicide is selected from the group consisting of chromium, cobalt, molybdenum, nickel, niobium, palladium, platinum, tantalum, titanium, tungsten, and vanadium.

34. The local interconnect of claim 32, wherein said first metal silicide comprises titanium silicide and said second metal silicide comprises tungsten silicide.

35. A local interconnect for connecting a first active semiconductor region to a second active semiconductor region on a substrate assembly, said first and second active semiconductor regions being separated by an insulating region, said local interconnect comprising:

a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide, said refractory metal from said first refractory metal silicide being different from said refractory metal from said second refractor metal silicide.

36. The local interconnect of claim 35, wherein said composite structure has a thickness in the range of about 700 Angstroms to about 1800 Angstroms.

37. A semiconductor device comprising:

a substrate assembly having at least one semiconductor layer;

at least one field effect transistor formed in said at least one semiconductor layer, said least one field effect transistor having a source, a drain and a gate; and

a local interconnect for connecting at least one of said source, said drain and said gate to another active area within said substrate assembly, said local interconnect comprising a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide.

38. A memory array comprising:

a plurality of memory cells arranged in rows and columns and formed on a substrate assembly having at least one semiconductor layer, each of said plurality of memory cells comprising at least one field effect transistor; and

at least one local interconnect for connecting at least one of a source, a drain and a gate of said at least one field effect transistor in one of said plurality of memory cells to one of an active area within said one memory cell or to one of a source, a drain and a gate of said at least one field effect transistor in another one of said plurality of memory cells, said local interconnect comprising a composite structure comprising a first refractory metal silicide, a second refractory metal silicide and an intermetallic compound comprising refractory metal from said first refractory metal silicide and refractory metal from said second refractory metal silicide.

39. The memory array of claim 38, further comprising a plurality of local interconnects for connecting additional active areas within each of said plurality of memory cells.

40. The memory array of claim 38, further comprising a plurality of local interconnects for connecting together active areas from different memory cells.

ABSTRACT OF THE DISCLOSURE

A process for forming a local interconnect includes applying a layer of metal over a semiconductor layer. A layer of metal silicide is formed over the layer of metal. The layer of metal silicide is patterned to define the boundaries of the local interconnect. The metal silicide is reacted with the layer of metal to form a composite structure. The composite structure includes the metal silicide, another metal silicide formed as silicon from the metal silicide reacts with the underlying layer of metal and an intermetallic compound of the metal from the layer of metal and metal from the layer of metal silicide. The unreacted layer of metal is removed with the composite structure remaining as the local interconnect.

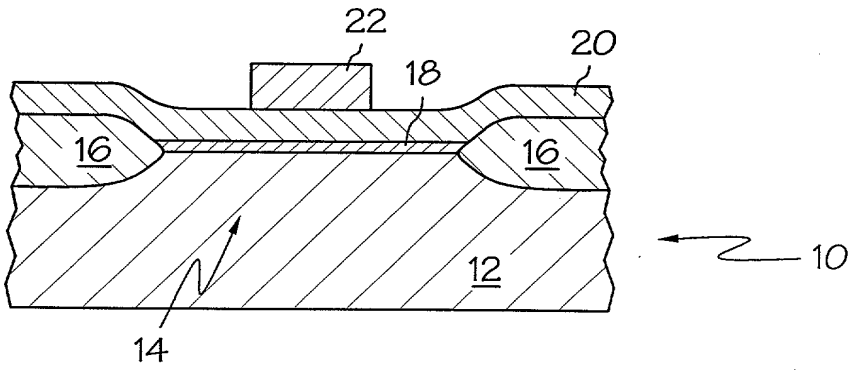

FIG. 1

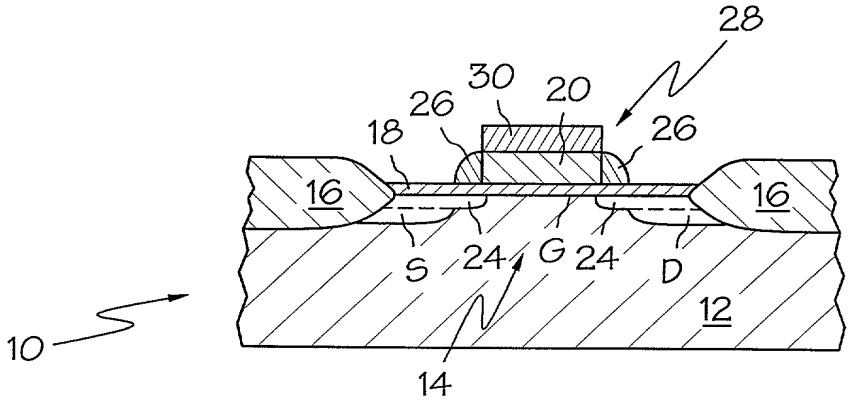

FIG. 2

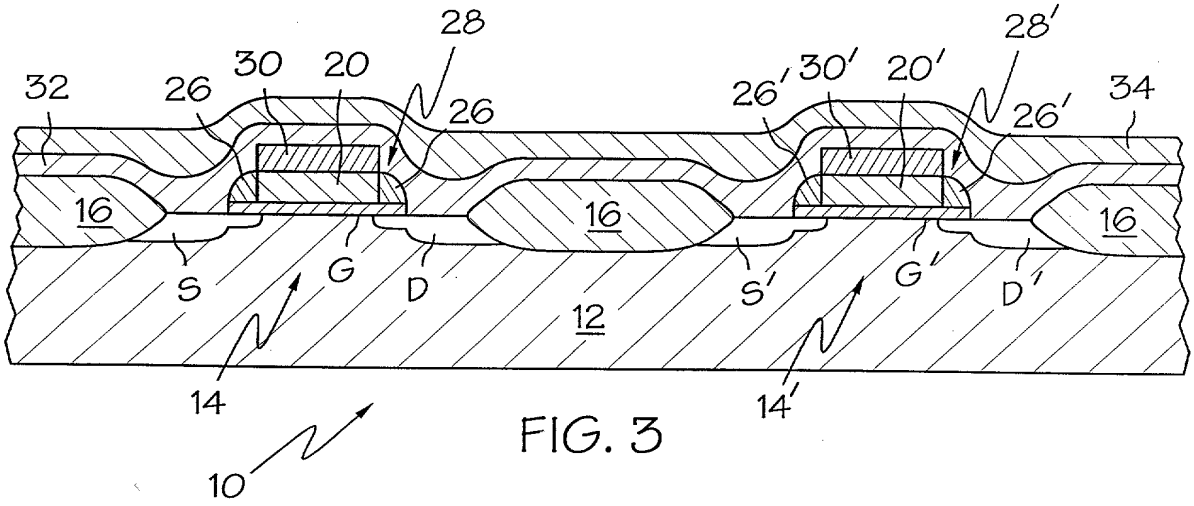

FIG. 3

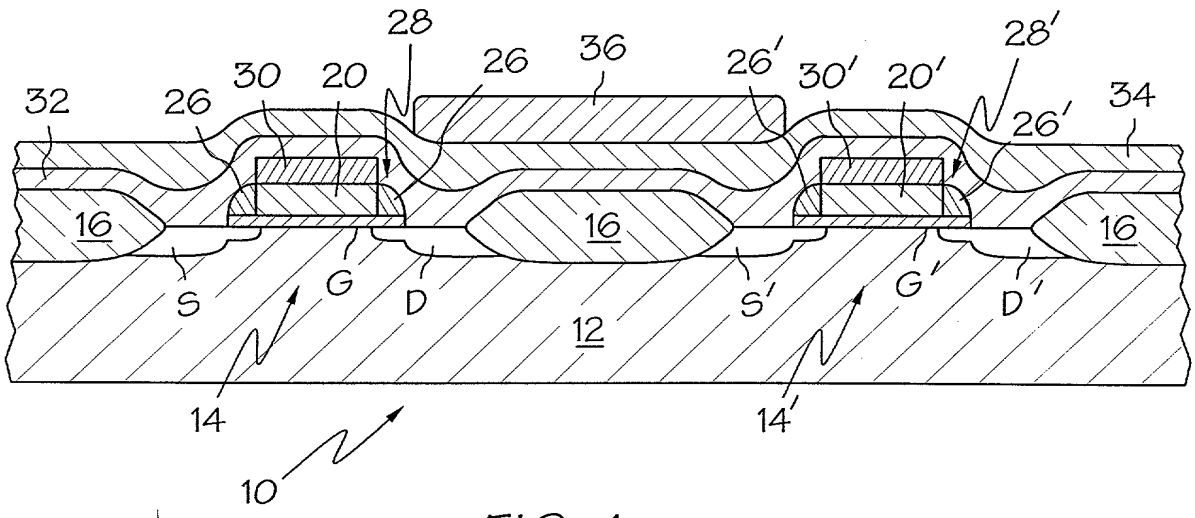

FIG. 4

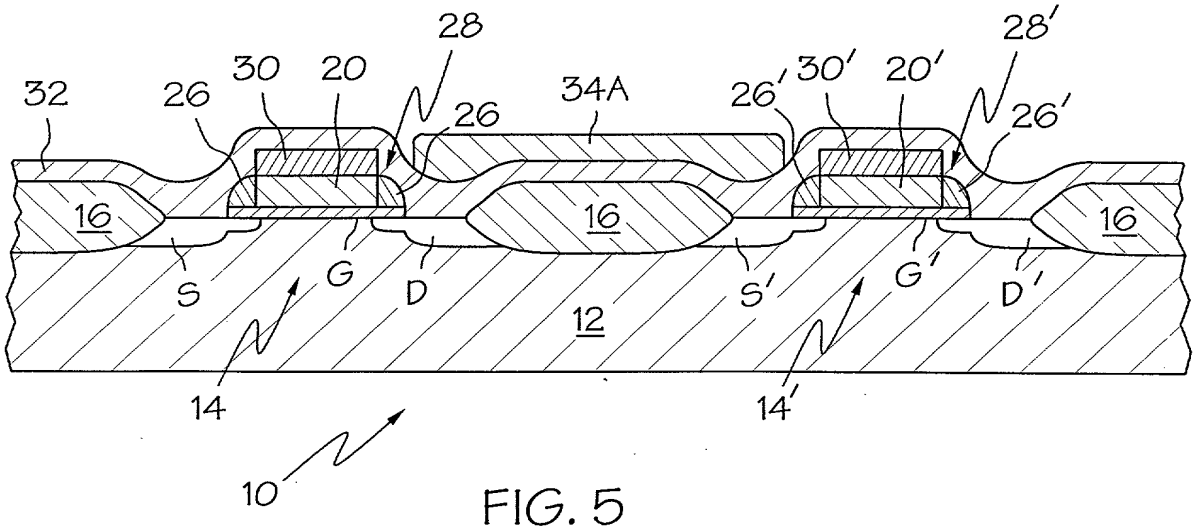

FIG. 5

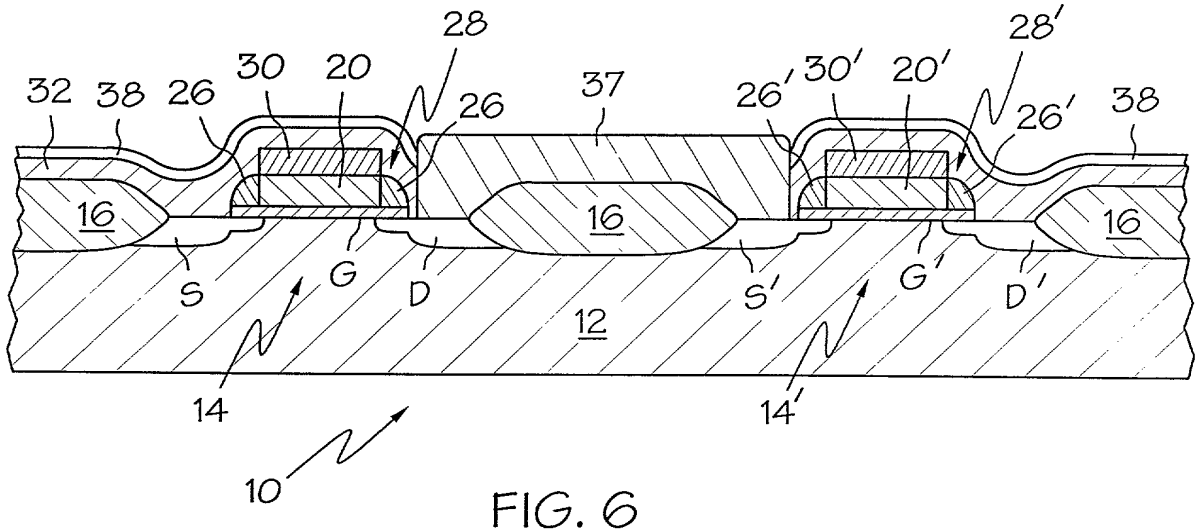

FIG. 6

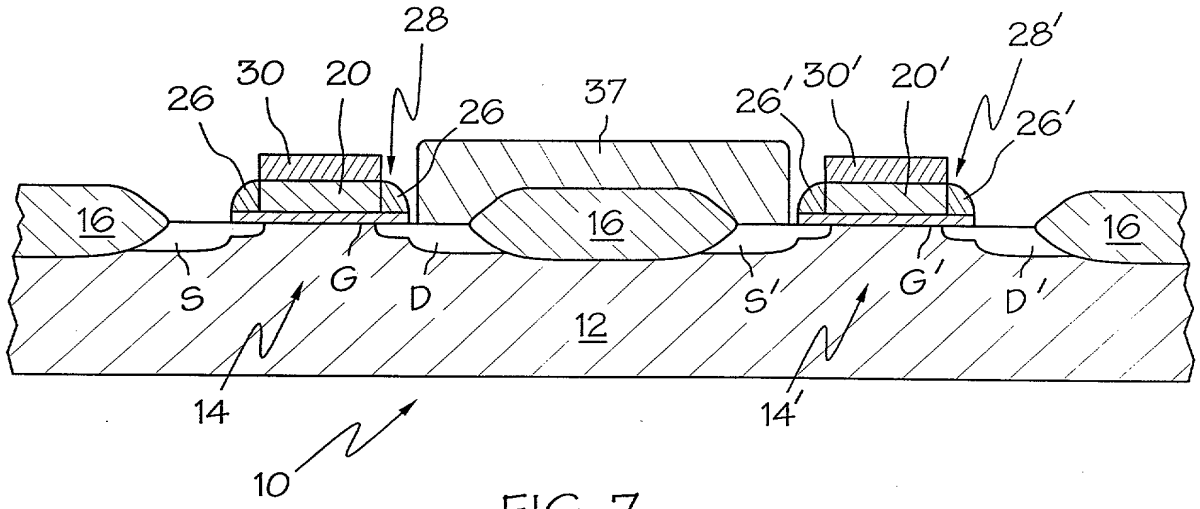

FIG. 7

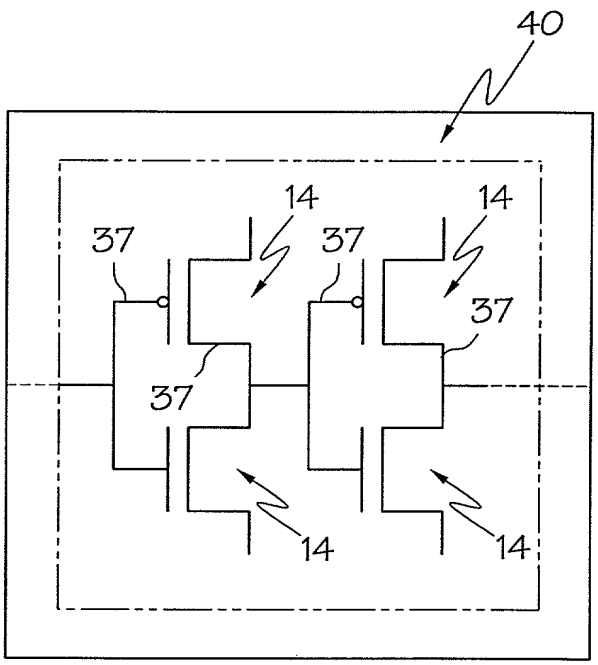

FIG. 8

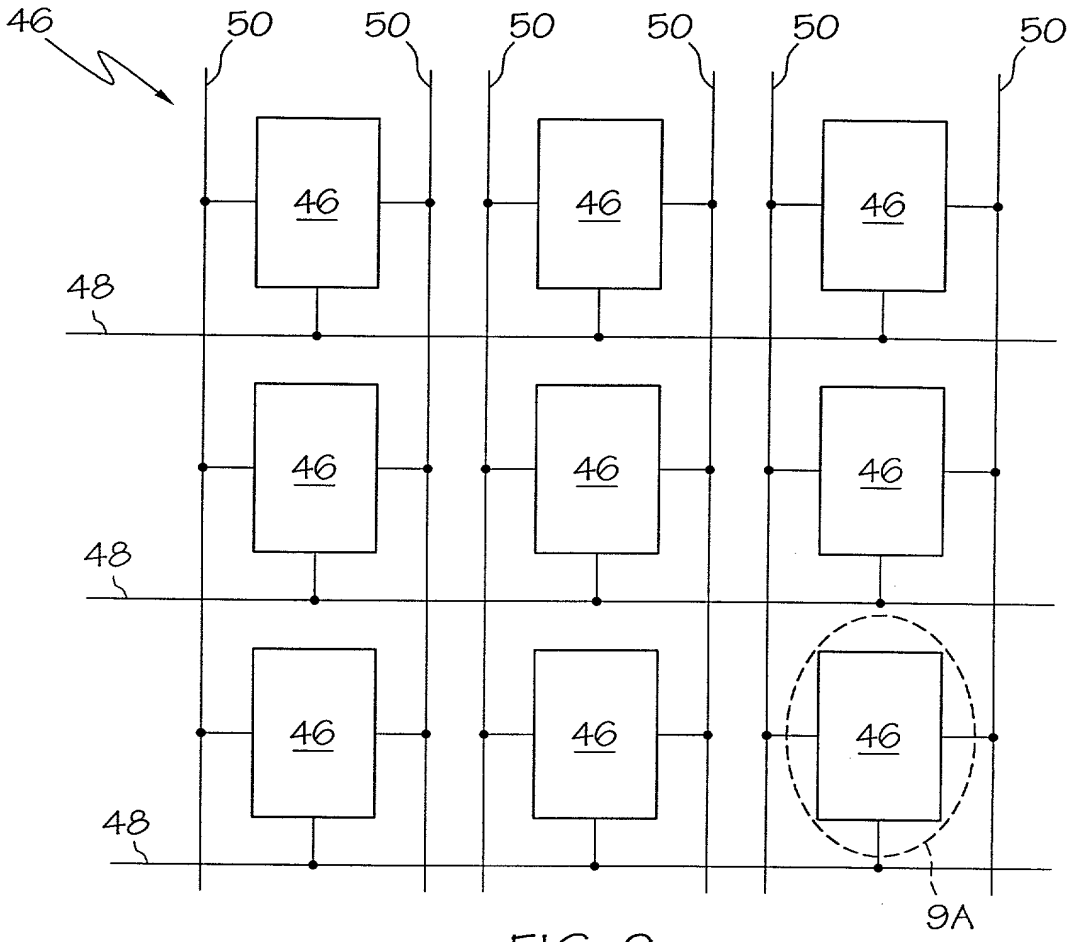

FIG. 9

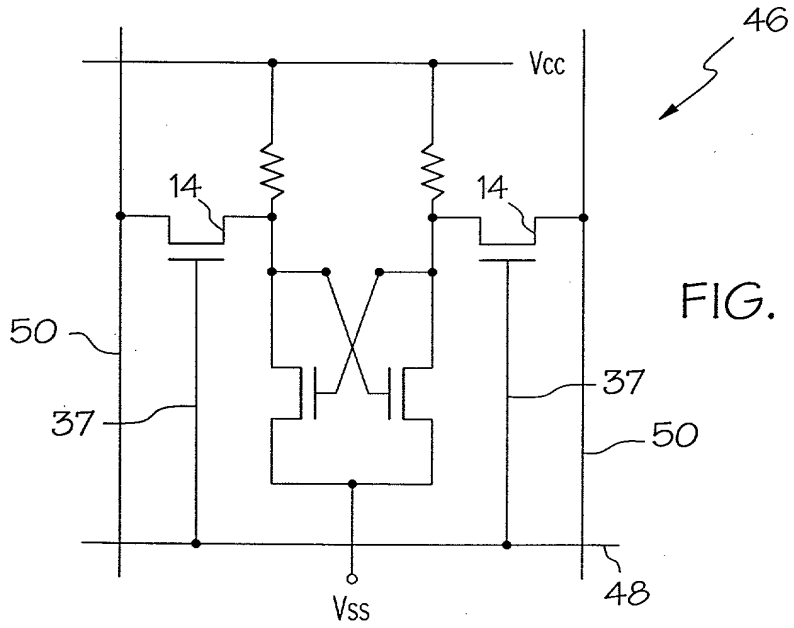

FIG. 9A

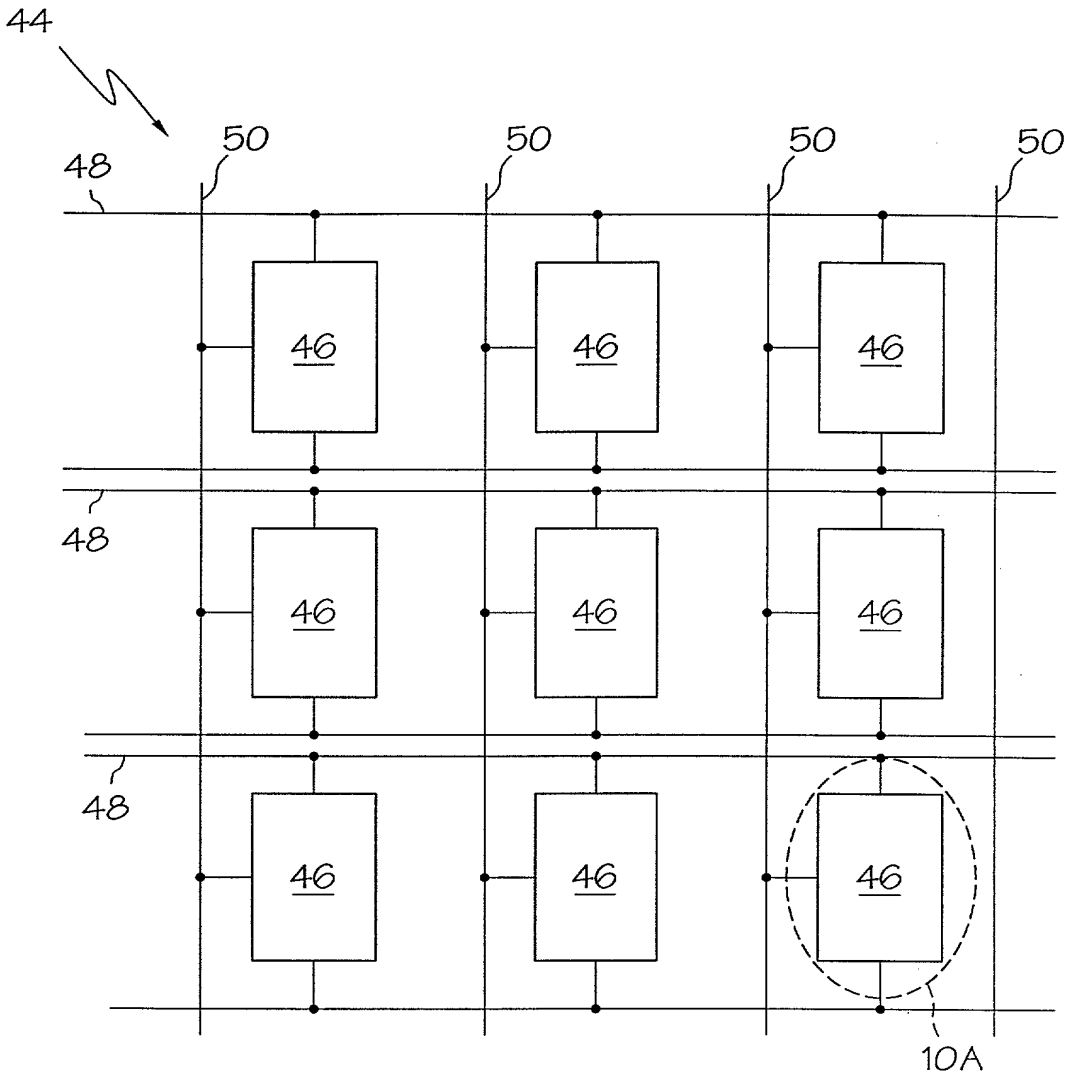

FIG. 10

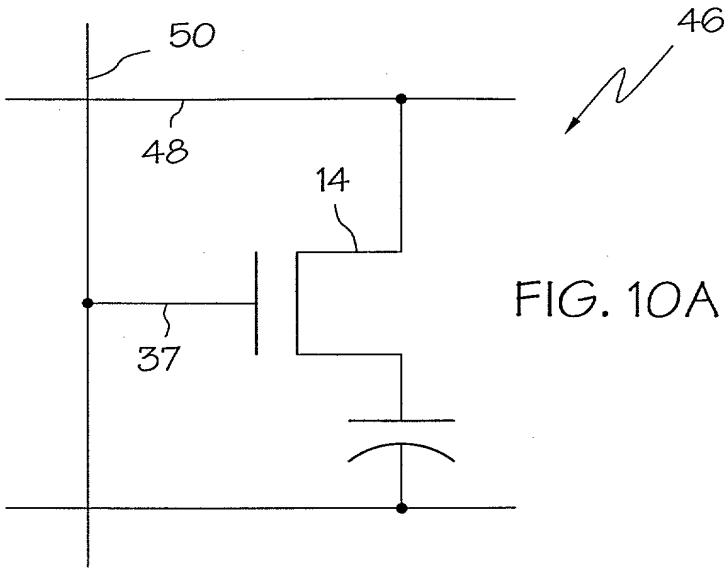

FIG. 10A

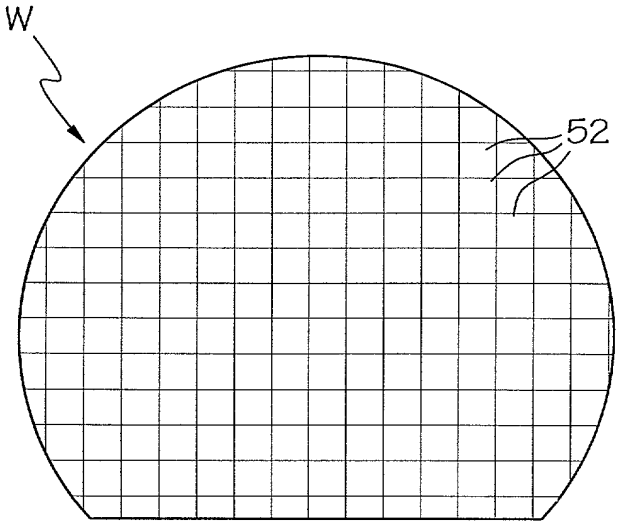

FIG. 11

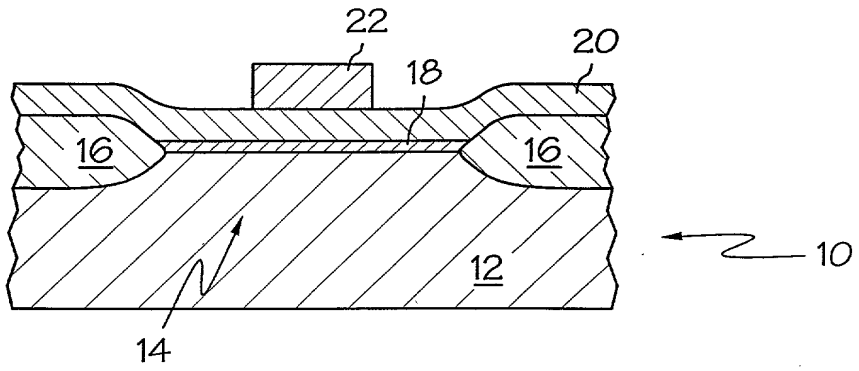

FIG. 1

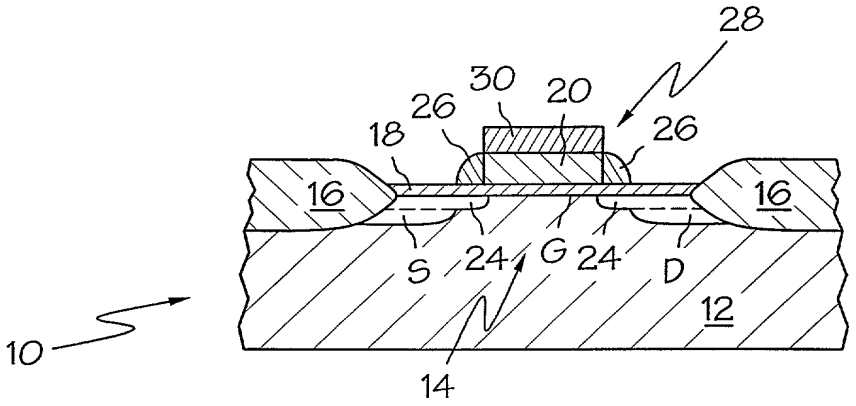

FIG. 2

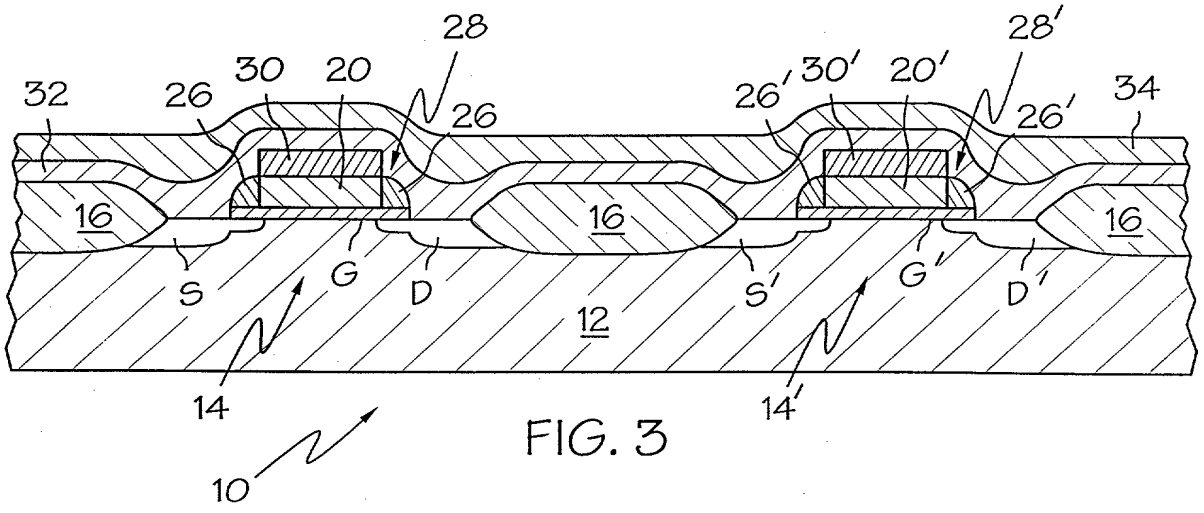

FIG. 3

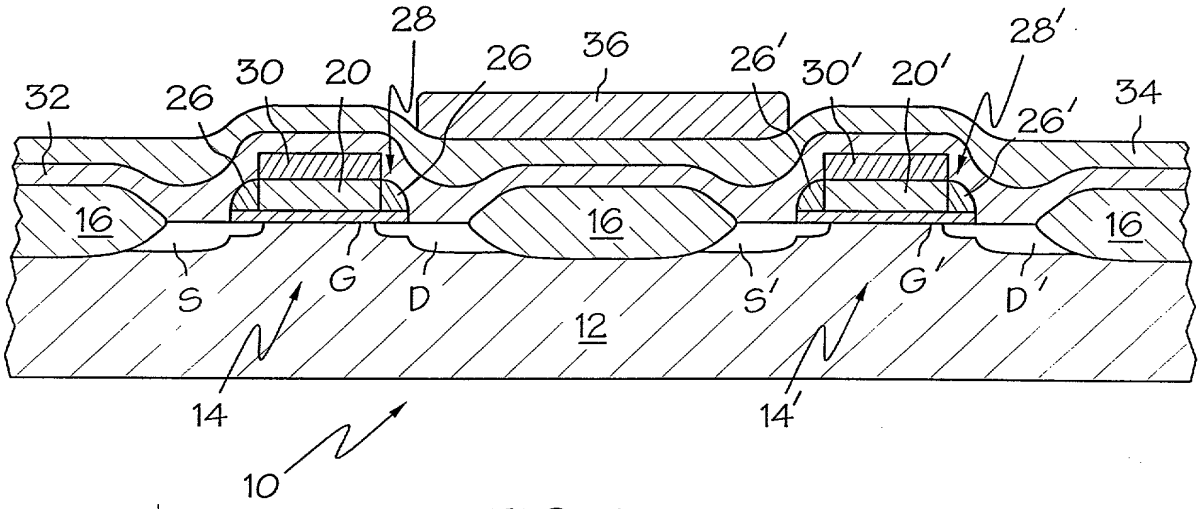

FIG. 4

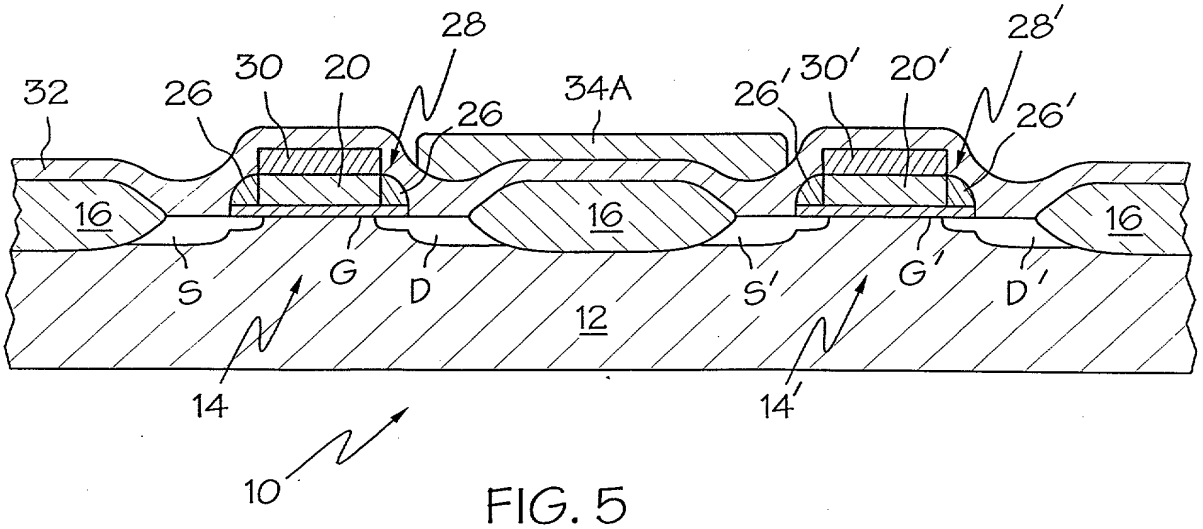

FIG. 5

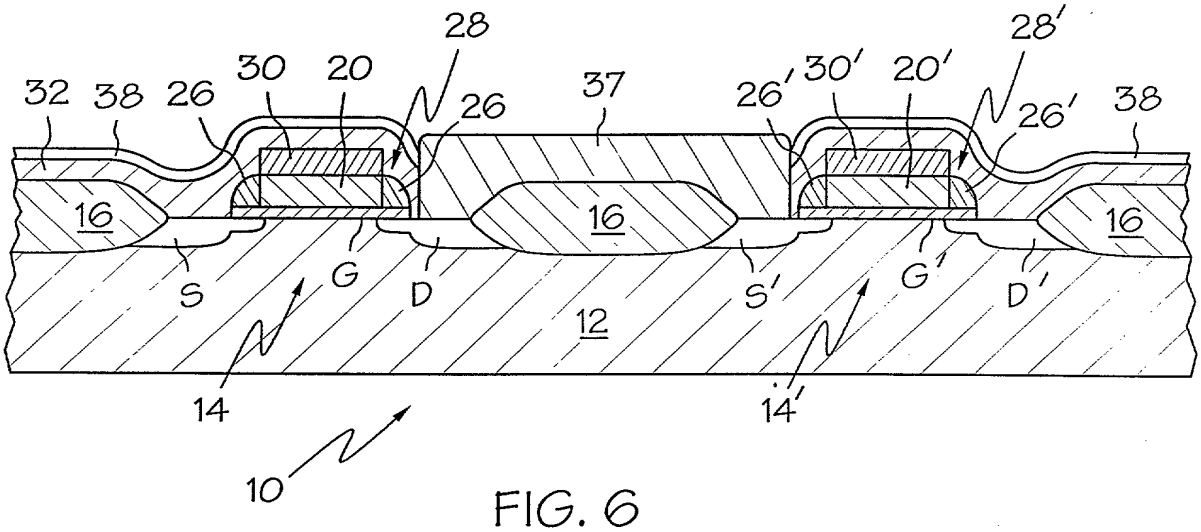

FIG. 6

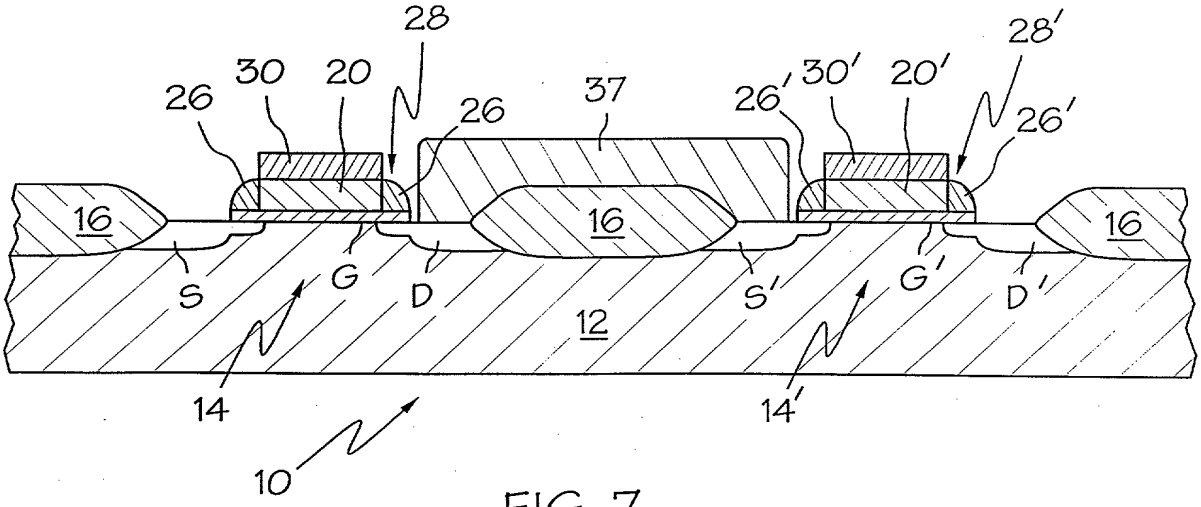

FIG. 7

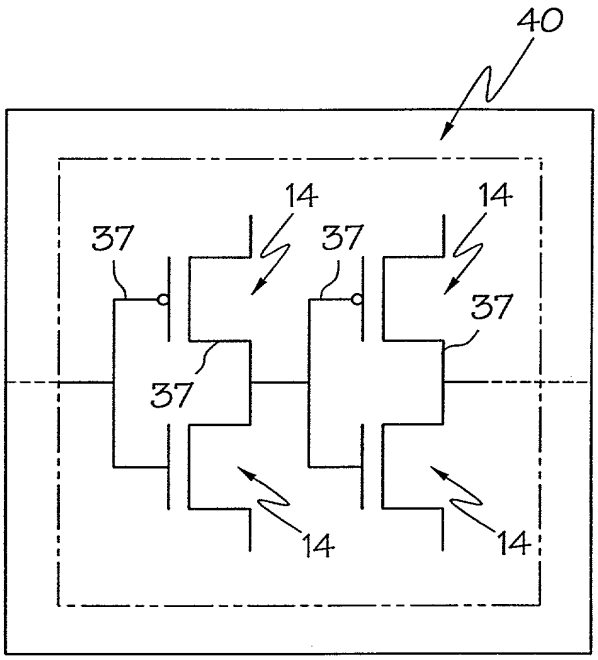

FIG. 8

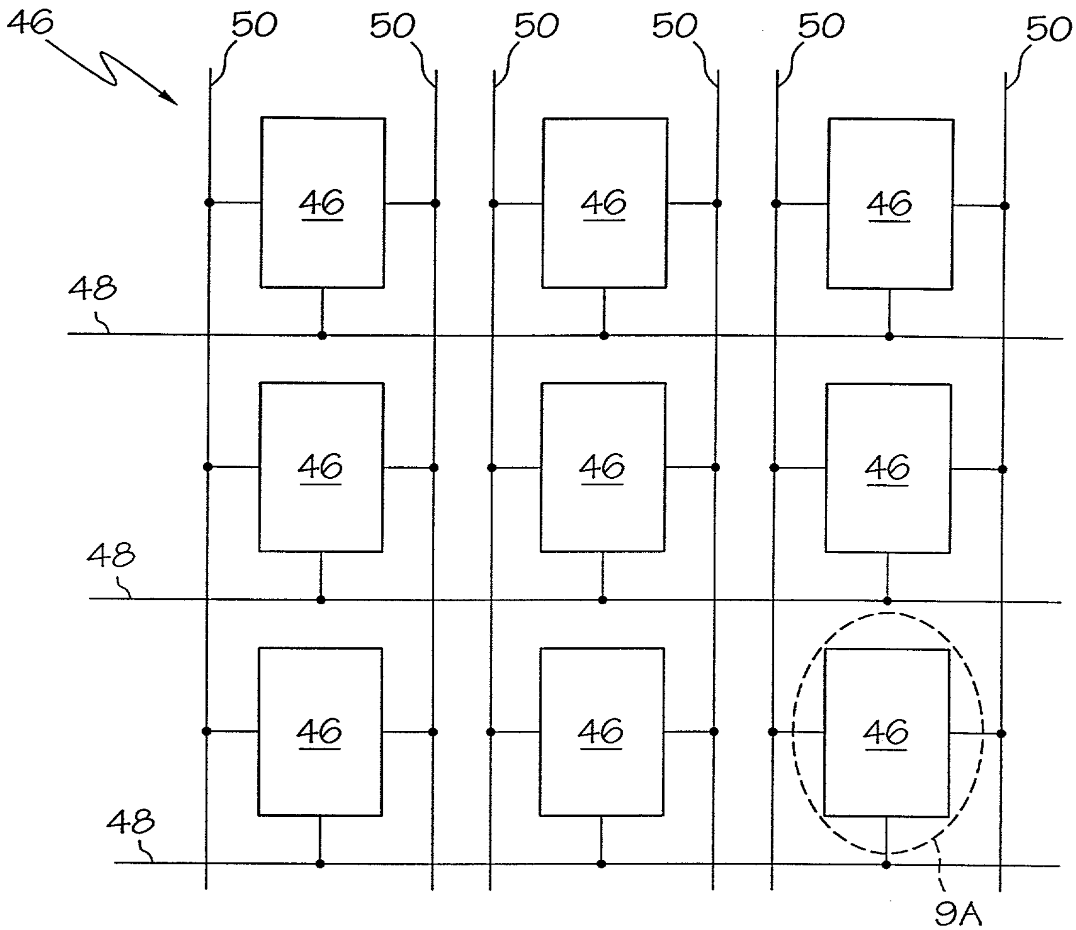
46
50
50
50
50
50
50
46
46
46
48
46
46
46
48
46
46
46
48
9A

FIG. 9

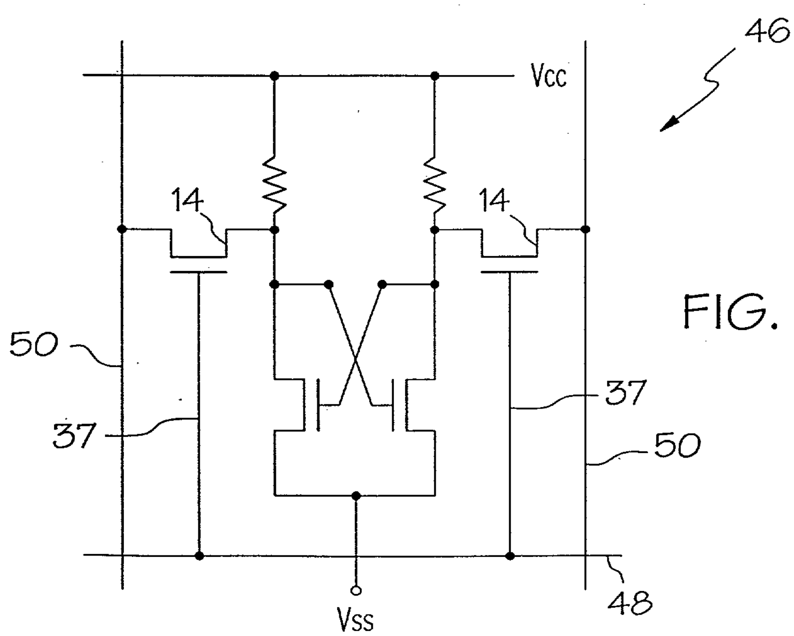
46
Vcc
14
14
50
37
37
50
48
Vss

FIG. 9A

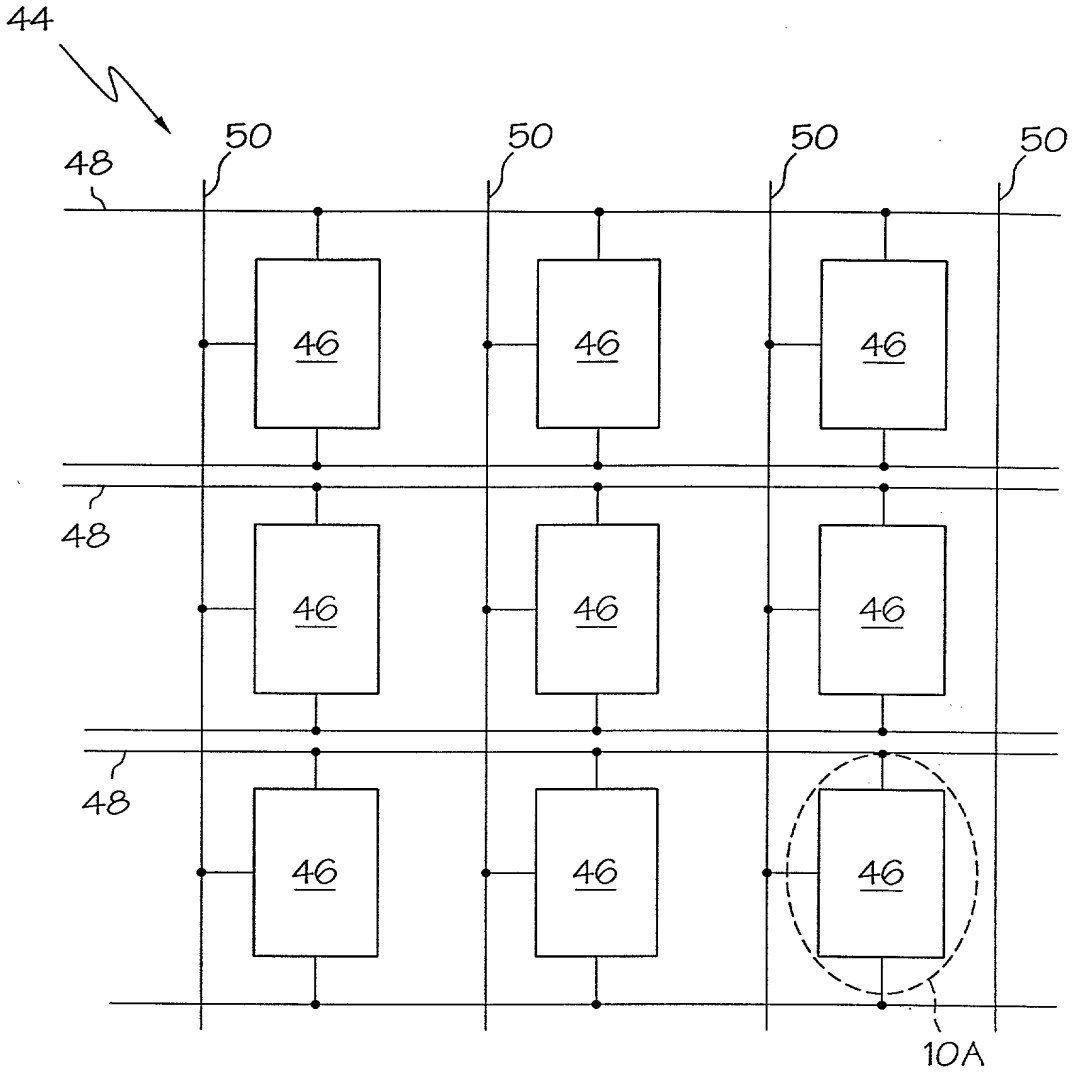

FIG. 10

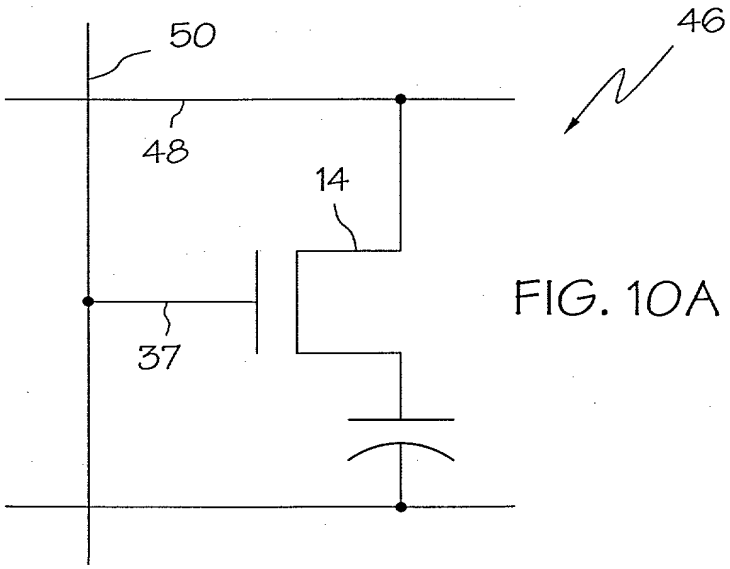

FIG. 10A

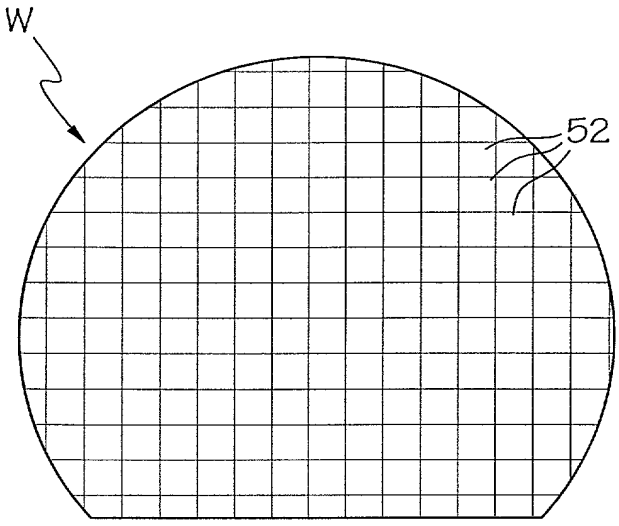

FIG. 11

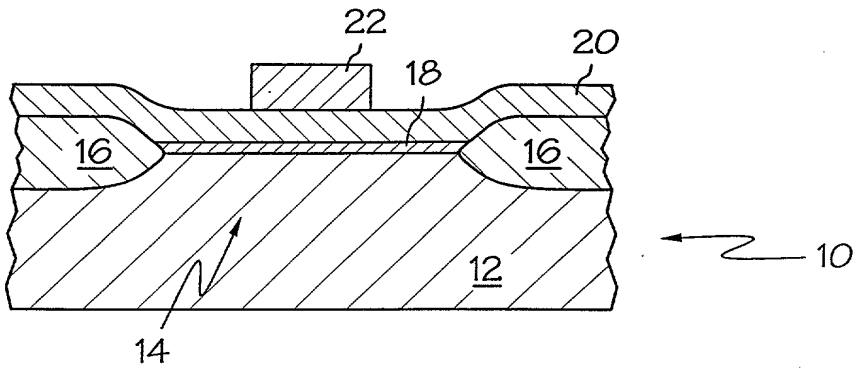

FIG. 1

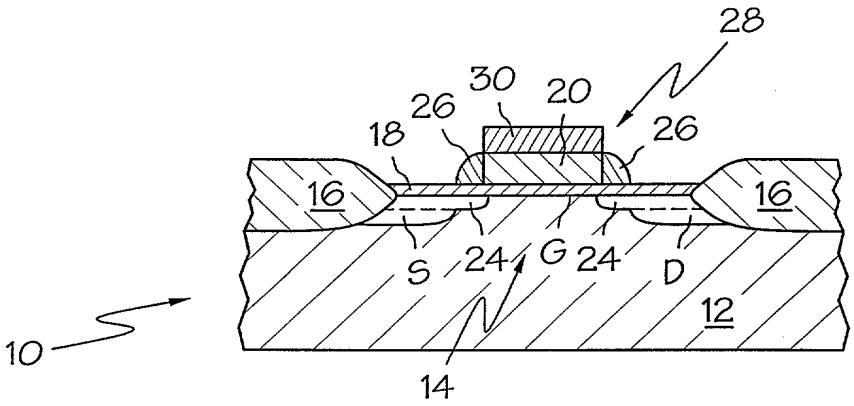

FIG. 2

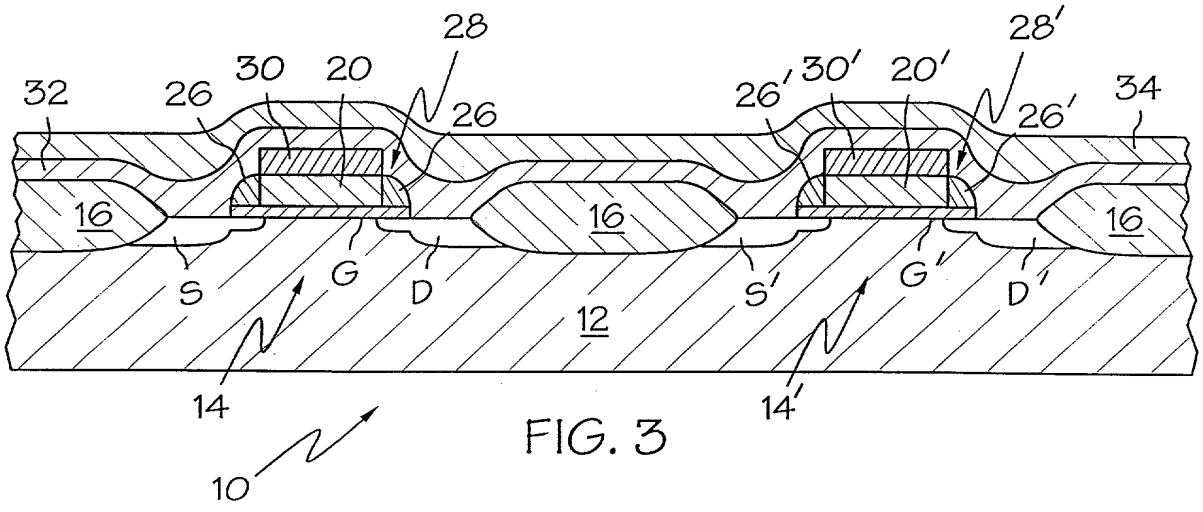

FIG. 3

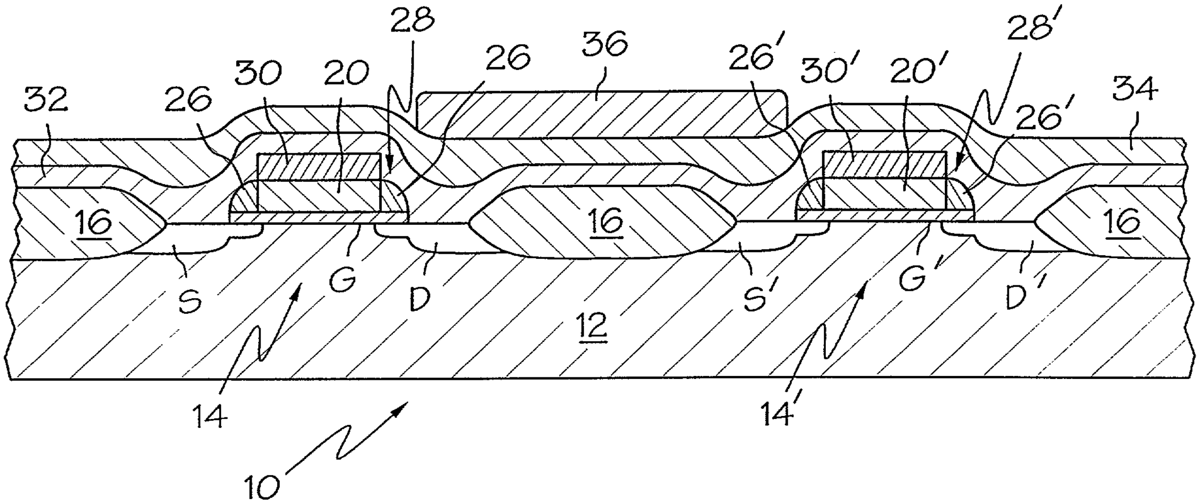

FIG. 4

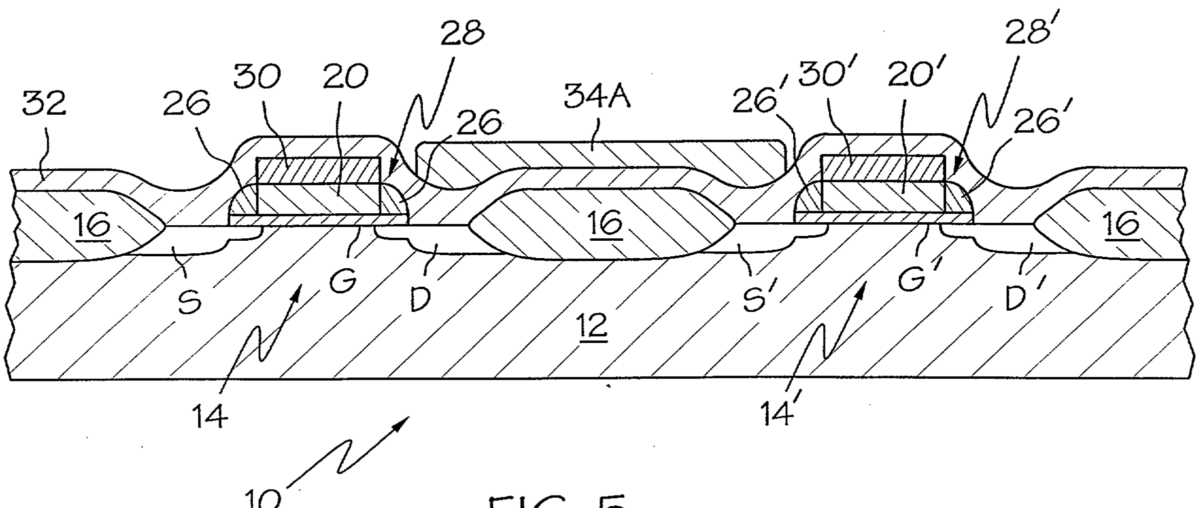

FIG. 5

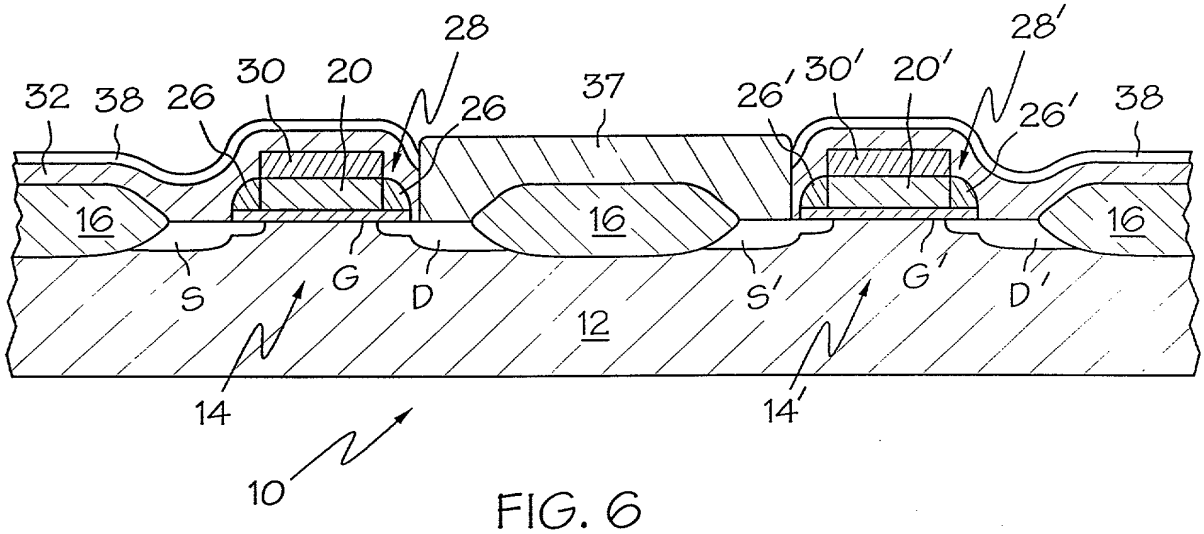
28
28′
32
38
26
30
20
26
37
26′
30′
20′
26′
38
16
16
16
S
G
D
S′
G′
D′
12
14
14′
10

FIG. 6

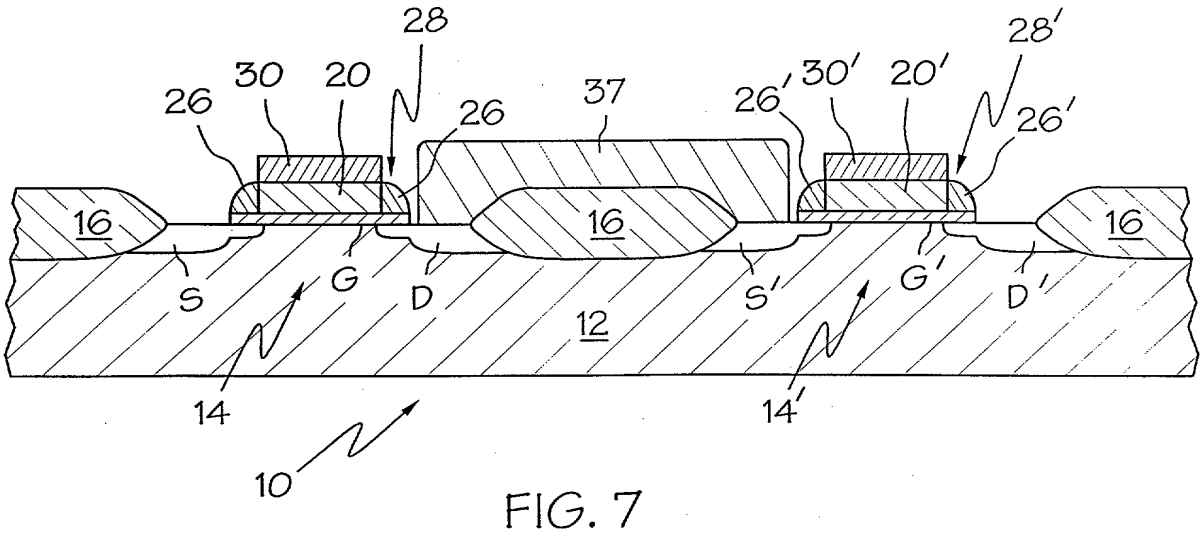
28
28′
26
30
20
26
37
26′
30′
20′
26′
16
16
16
S
G
D
S′
G′
D′
12
14
14′
10

FIG. 7

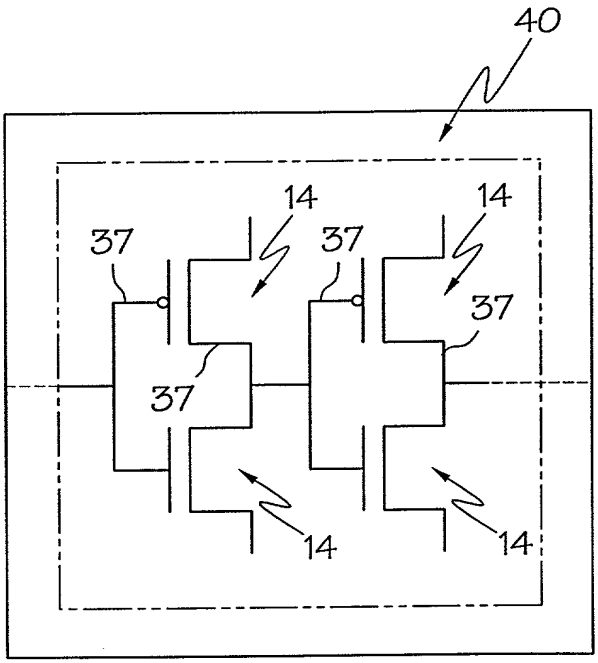

FIG. 8

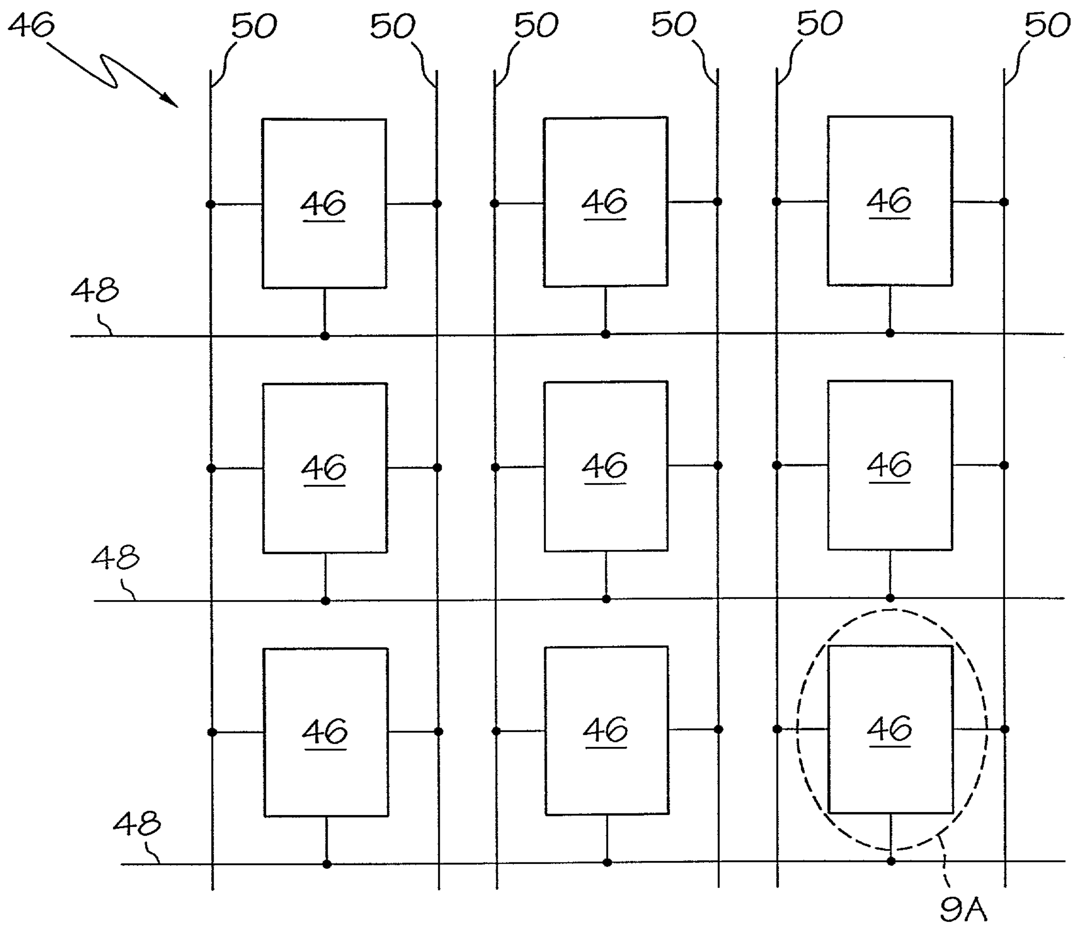
46
50
50
50
50
50
50
46
46
46
46
46
46
46
46
46
48
48
48
9A

FIG. 9

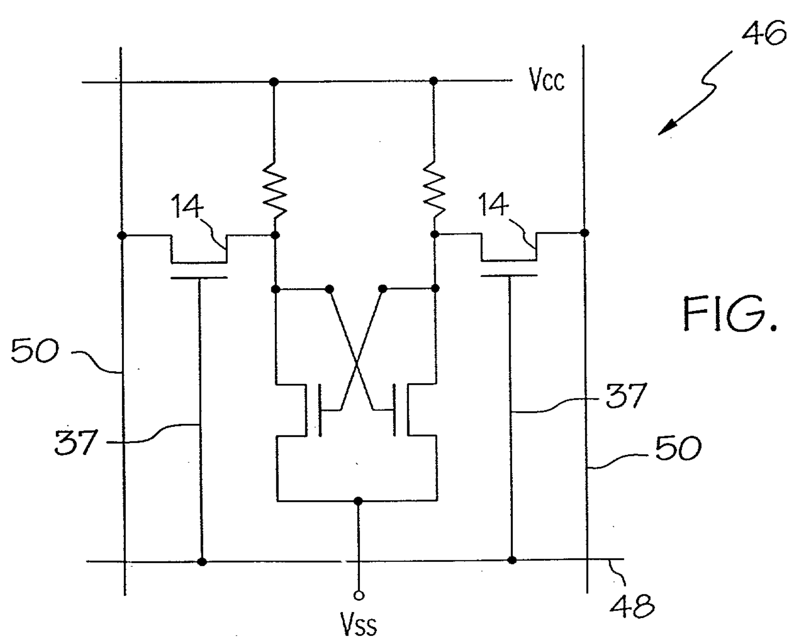
46
Vcc
14
14
50
37
37
50
48
Vss

FIG. 9A

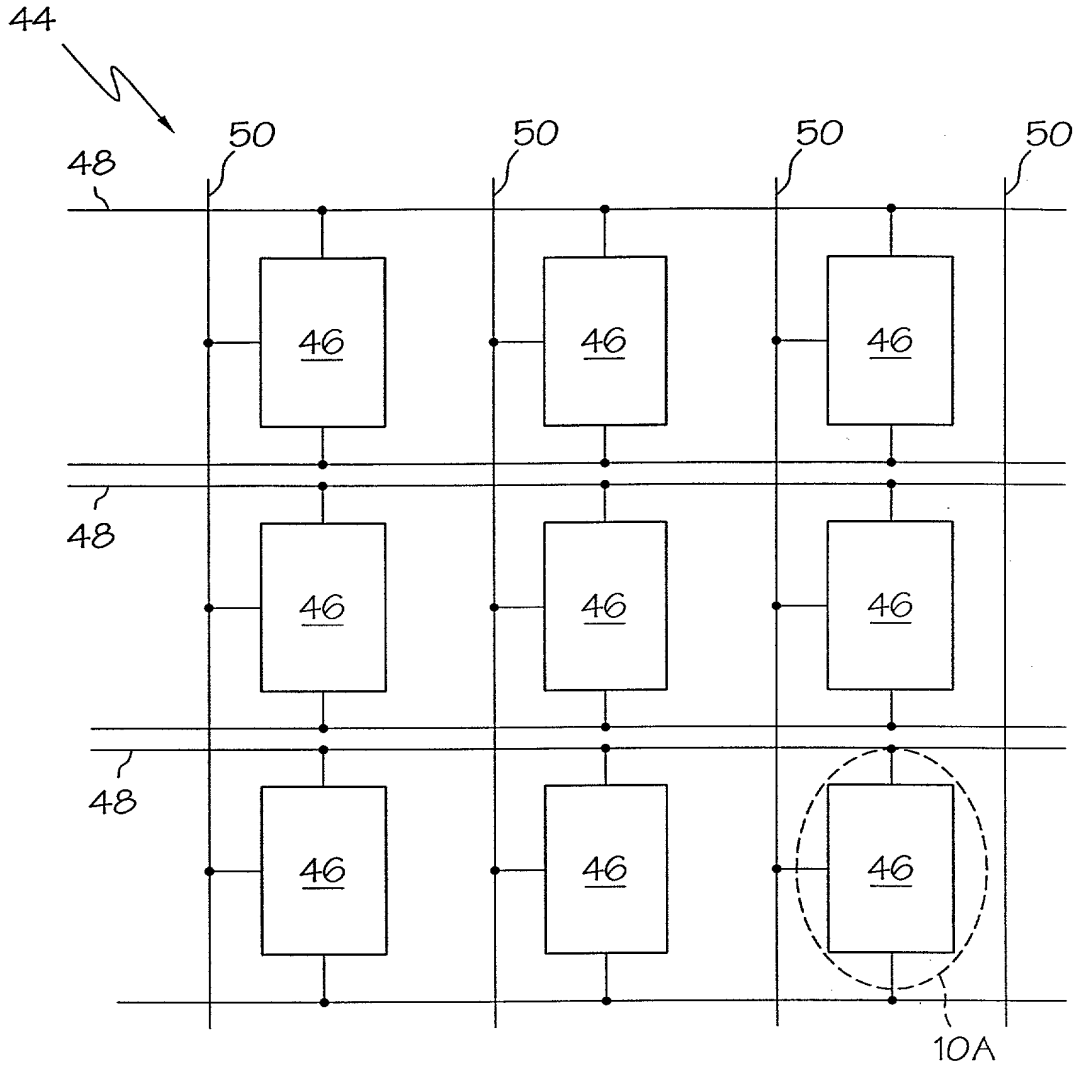

FIG. 10

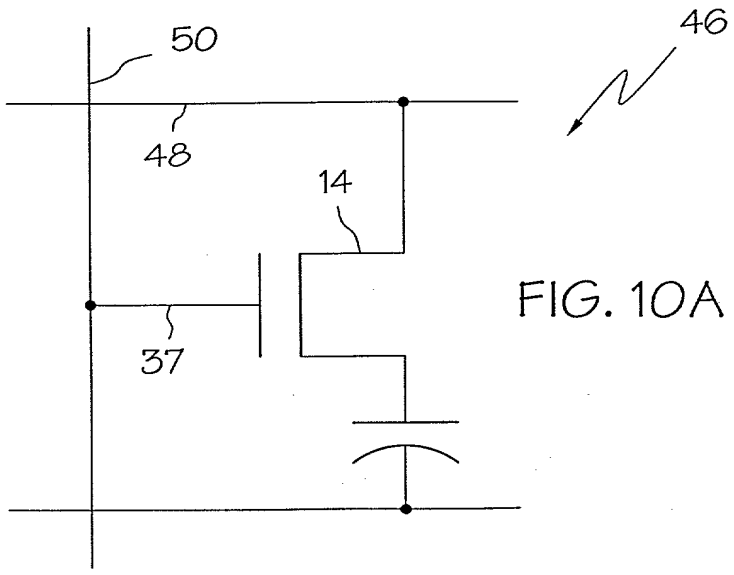

FIG. 10A

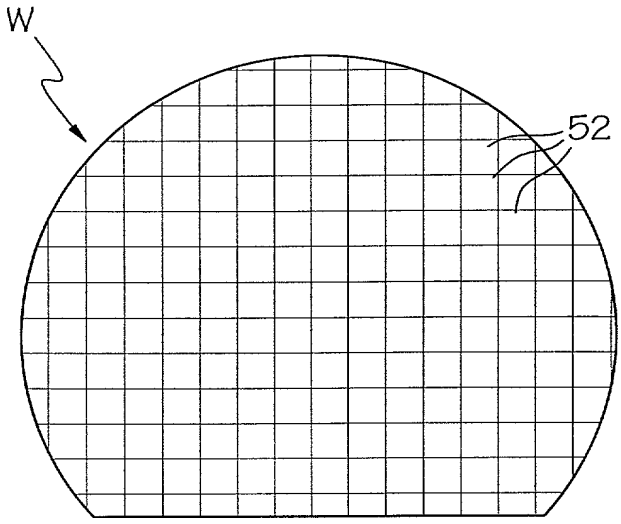

FIG. 11

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled:

LOW RESISTANCE METAL SILICIDE LOCAL INTERCONNECTS AND A METHOD OF MAKING, described and claimed

__X__ in the attached specification;
______ in the specification filed ______________________________,
as U.S. Application Serial No. ________________, and as amended ______________________________.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as filed and as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56(a).

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Richard A. Killworth	Reg. No. 26,397
James F. Gottman	Reg. No. 27,262
Timothy W. Hagan	Reg. No. 29,001
Richard C. Stevens	Reg. No. 28,046
Robert L. Showalter	Reg. No. 33,579
Susan M. Luna	Reg. No. 38,769
James E. Beyer	Reg. No. 39,564
Bradley A. Keller	Reg. No. 37,654
Charlotte L. Barney	Reg. No. 35,060
W. Bryan Farney	Reg. No. 32,651
Michael L. Lynch	Reg. No. 30,871
Lia M. Pappas	Reg. No. 34,095

Address all telephone calls to (937) 223-2050. Address all correspondence to: KILLWORTH, GOTTMAN, HAGAN & SCHAEFF, L.L.P., One Dayton Centre, One South Main Street, Suite 500, Dayton, Ohio 45402-2023.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of sole or first Inventor: Jigish D. Trivedi

Inventor's signature Jigish D. Trivedi

Date: 08/20/97

Residence: 197 E. Mallard Drive
Apt #231
Boise, Idaho 83706

Citizenship: India

Post Office Address: c/o Micron Technology, Inc.
8000 S. Federal Way
Boise, ID 83706-9632